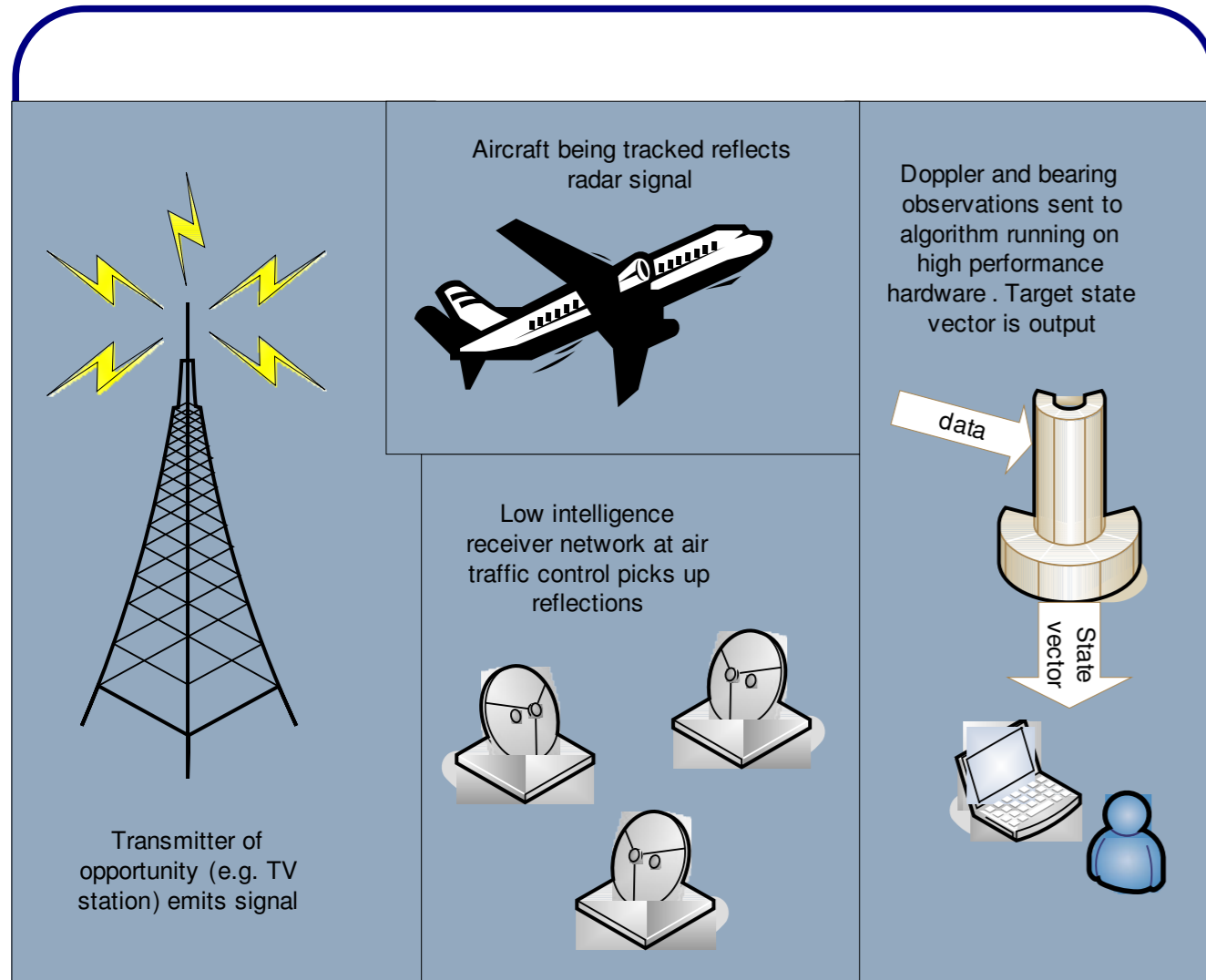


High Performance Computing Applied to Multiple Target Tracking Using Doppler and Bearing Data

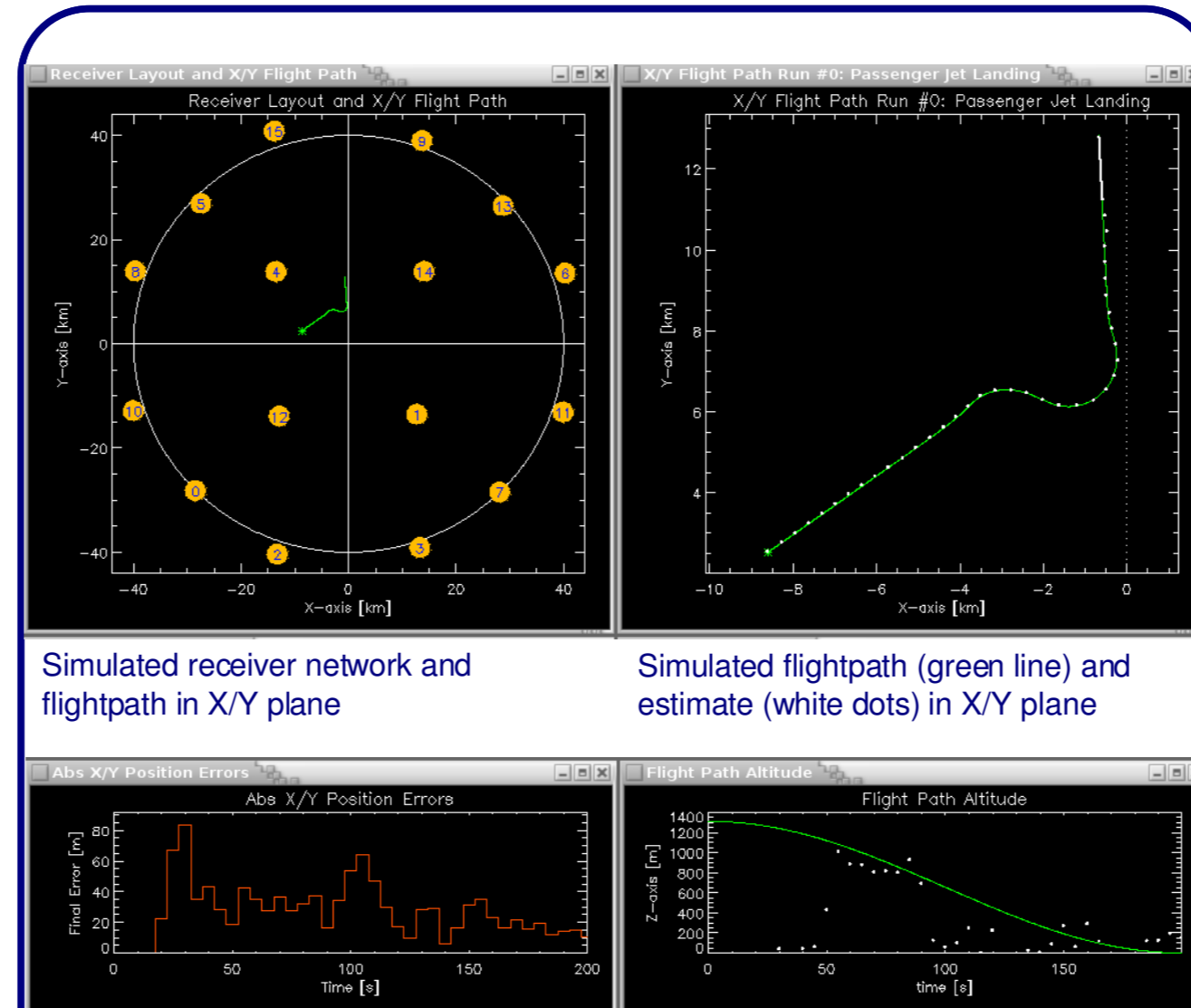
AIM: To parallelize a filtering algorithm for tracking single targets in order to simultaneously track multiple aircraft

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Air Traffic control with the PCL system

- The algorithm, developed by Dr Norman Morrison, uses non-linear differential correction to develop a state vector for a target using doppler and bearing data as input.
- The algorithm is suitable for a low cost Passive Coherent Location (PCL) system which could be an option for air traffic control in developing countries.
- Input is fed into an Expanding Memory Polynomial filter of degree 1 for initialization. EMP filtering finds the straight line that best fits the observations in the sense of least squares.
- The state vector developed from the smoothed data specifies position and velocity in two dimensions.
- After initialization, control is passed to the differential correction algorithm. The model uses a polynomial of either degree 1 or 2.
- The state vector developed specifies position, velocity and acceleration in three dimensions.



X/Y Position error histogram Flight path altitude with estimate
Above Screenshots taken from PCL Simulator developed by Dr Richard Lord

$$X(t) = \begin{pmatrix} x_0 \\ x_1 \\ x_2 \\ \dots \\ x_3 \\ x_4 \\ x_5 \\ \dots \\ x_6 \\ x_7 \\ x_8 \\ \vdots \end{pmatrix}_t = \begin{pmatrix} x \\ \dot{x} \\ \ddot{x} \\ \dots \\ y \\ \dot{y} \\ \ddot{y} \\ \dots \\ z \\ \dot{z} \\ \ddot{z} \\ \vdots \end{pmatrix}_t$$

State Vector

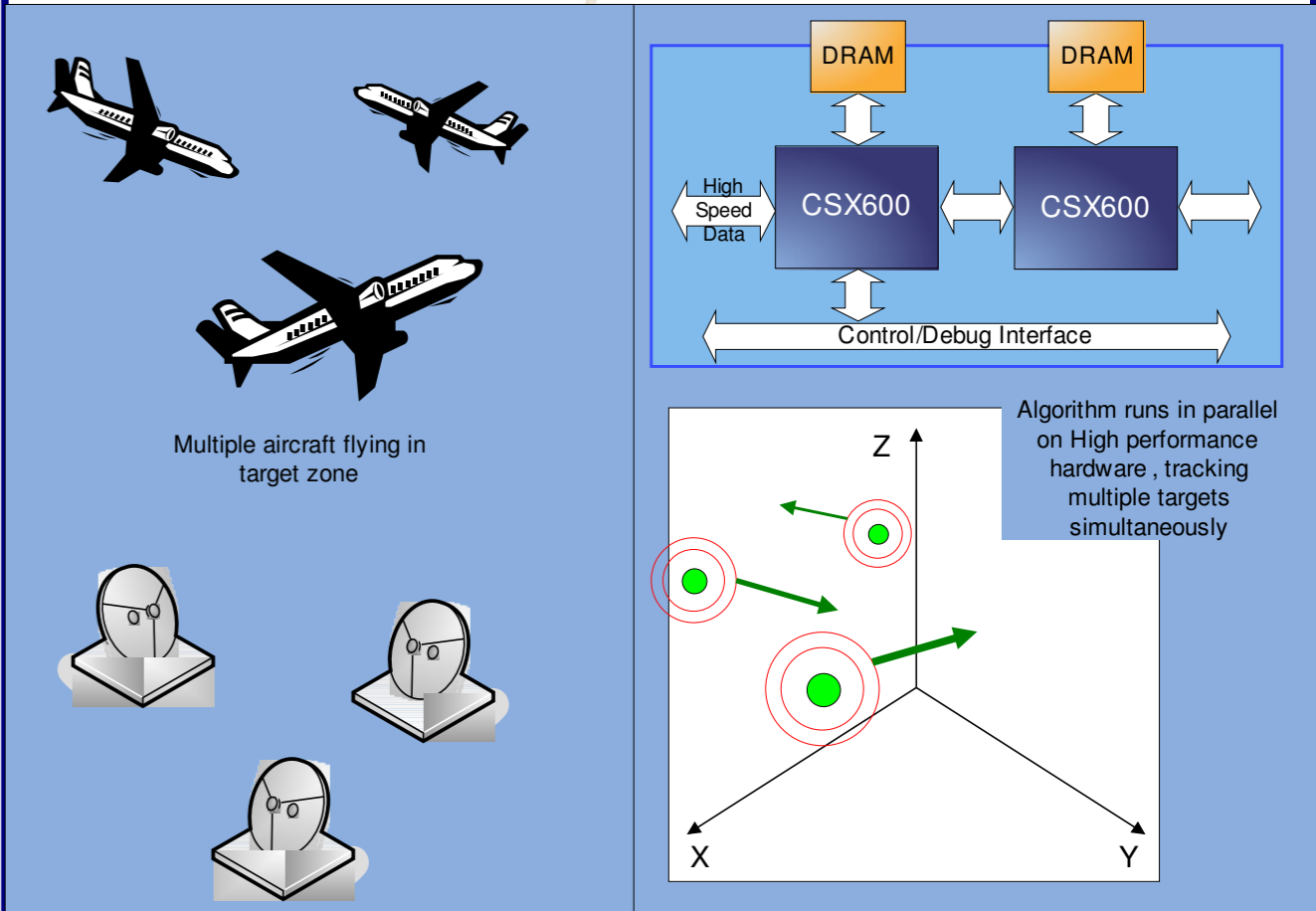
•Research objectives:

- Test the algorithm under more realistic conditions using a more sophisticated radar simulator.
- Accelerate the computationally intensive sections of the code on high performance hardware.
- Parallelize the algorithm in order to track multiple targets simultaneously

•Differential correction combines data from a number of radar receivers using the minimum variance rule. New data is incorporated as it is received in order to continually correct the model in an optimal fashion.

•The algorithm is computationally intensive and involves high dimension matrix inversions and matrix-matrix multiplication.

Clearspeed's Advance Board with CSX600 processor & PCI-X form factor



Proposed parallelization of algorithm on CSX600 Advance

- Proposed Hardware: Clearspeed Advance CSX600 Accelerator.
- CSX600: A massively parallel embedded processor aimed at accelerating compute intensive simulations.
- Advance board: 2 CSX600s, FPGA with sequential data path, PCIe or PCIX form factor. The board slots into a general purpose CPU
- The board is capable of 50GFLOPS sustained DGEMM at 25W.
- It is programmed in C, and supports Level 3 BLAS, FFTW and LAPACK.
- Code is enabled to run on the CSX600 by making Clearspeed library function calls.
- The runtime environment uses heuristics to determine how to split processing between the host CPU and the advance accelerator card.



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