A 500kHz - 5MHz CW Stepped Frequency Borehole Tomographic Imaging System

Adam Rhett Isaacson

A dissertation submitted to the Department of Electrical Engineering,
University of Cape Town, in fulfilment of the requirements
for the degree of Master of Science in Engineering.

Cape Town, December 2002

Declaration

I declare that this dissertation is my own, unaided work. It is being submitted for the degree of Master of Science in Engineering in the University of Cape Town. It has not been submitted before for any degree or examination in any other university.

Signature of Author .....

Cape Town
1 December 2002

Abstract

Professor Iain Mason, of the University of Sydney, De Beers, and Reutech Radar Systems sponsored the Radar Remote Sensing Group at UCT to develop a prototype, CW, Stepped Frequency, Borehole, Tomographic Imaging System, proposed by Dr. Alan Langman, of the University of Cape Town. The system is to demonstrate that a coherent system can be achieved using DDS technology.

This dissertation involves a study of Cross-Borehole Tomography. The mathematical physical models of the Radon Transform are reviewed. The entire Cross-Borehole Tomographic process is simulated, based on these physical models of the Radon Transform. The system specifications for the final design are based on the results from the simulation. Finally, the final design is built, and tested.

The phase yields a better quality of image reconstruction when compared to amplitude, and hence a coherent system is a good choice. The system is frequency to frequency coherent for the entire transmit frequency range, which satisfies the main aim of this dissertation.

To my mother, and in memory of my father

Godfrey Julius Isaacson

1936–1994

Acknowledgements

I would like to thank the following people who helped bring about this dissertation:

- My supervisor, Professor M. R. Inggs, for his help, assistance, and valued support during this dissertation.
- Dr. Alan Langman, for his enthusiasm, moral support, and his many suggestions during this dissertation.
- Professor Iain Mason, for his financial support, and interest in this dissertation.
- De Beers for their financial support.
- Reutech Radar Systems, for their financial support, and use of their facilities during this dissertation. A special mention to Chris May, Bryn Jones, Pieter-Jan Wolfaardt, Paul Fourie, PW van der Walt, and Sven Holfelder. Thanks guys, your support was most appreciated!
- Finally, I would like to thank my mom, and my girlfriend, Gina, for their moral support. Love you both!

Contents

List of Figures

List of Tables

List of Symbols

A_{pq}	—	Amplitude of signal along ray path pq.
c	—	Speed of light.
d_i	—	Amplitude or traveltime for the ith ray path.
E_{pq}	—	Electric field of the EM wave along ray path pq.
E_o	—	Initial electric field constant.
f	—	Transmit frequency.
k	—	Angular wave number.
l_{ij}	—	Length of the ith ray that passes the jth pixel.
$L_{unambig}$	—	Unambiguous path length.
N	—	Number of bits of the ADC.
p_j	—	Attenuation or the velocity for the pixel j.
P_{1dB}	—	1dB compression point of the LNA.
P_{min}	—	Minimum detectable signal within the receiver bandwidth.
T_{pq}	—	Traveltime along ray path pq.
v	—	Velocity of travelling wave.
X_m	—	Full-scale amplitude of the ADC.
α	—	Attenuation constant.
β	—	Phase constant.
Δf	—	Frequency step size.
$\Delta\phi$	—	Change in phase.
ϵ_r	—	Relative permittivity.
$\epsilon^{'}$	—	Real part of permittivity.
$\epsilon^{''}$	—	Imaginary part of permittivity.
λ	—	Wavelength.
μ	—	Permeability.
σ	—	Conductivity.
σ_x	—	RMS amplitude value of the input ADC signal.
ω	—	Angular frequency.

Nomenclature

Coherent System—A system where the phase information is preserved.

CW—Continuous Wave.

IF—Intermediate Frequency.

BPF—Band Pass Filter.

ADC—Analogue-to-Digital Converter.

COTS—Commercial off the Shelf.

DDS—Direct Digital Synthesiser.

Cross Borehole Tomography—A process which uses a transmitter, and a receiver in each borehole in order to obtain an image of the subsurface between the two boreholes.

EM Wave—Electromagnetic Wave.

Relative Permittivity—The ratio of the electric displacement in a medium to that which would be produced in free space by the same field.

Bakelite—A synthetic resin made by condensation of cresol or phenol with formaldehyde.

Magnetic Permeability—The ratio of flux density to magnetising force.

Conductivity—Reciprocol of the resistivity.

Homogenous Medium—The characteristics of the medium remain the same, and do not depend on position.

SVD—Singular Value Decomposition.

LSQ Error—Least Squares Error.

SNR—Signal-to-Noise Ratio.

LNA—Low Noise Amplifier.

IF Sampling Algorithm—This algorithm extracts the phase from the IF signal by using four IF samples to generate the I, and Q values, and hence the phase can be calculated.

Quantization Error—This is the error associated with the ADC. The ADC is essentially a quantizer, which transforms the actual sample values into a set of prescribed values. The difference between the prescribed values, and the actual sample values represents the quantization error.

PCB—Printed Circuit Board.

Flicker Noise—This is also called pink noise. It is defined as having a $\frac{1}{f}$ spectrum.

Baud Rate—The number of clock periods per second.

CPLD—Complex Programmable Logic Device.

UART—Universal Asynchronous Receiver Transmitter.

PC—Personal Computer.

DAC—Digital-to-Analogue Converter.

Chapter 1

Introduction

1.1 Background

Professor Iain Mason, of the University of Sydney, De Beers, and Reutech Radar Systems sponsored the Radar Remote Sensing Group[1] at UCT to develop a prototype, CW, Stepped Frequency, Borehole, Tomographic Imaging System, proposed by Dr. Alan Langman, of the University of Cape Town. The system is to demonstrate that a coherent system can be achieved using DDS technology. Most current borehole radar systems pulse a resonant, damped antenna to achieve ultra wide band (UWB) operation[2]. The Geosonde system developed by Mason at Oxford and Sydney covers the band 20 to 80MHz[3]. A stepped frequency system is a more flexible approach, possibly allowing for more efficient, automatically tuned antenna structures. In addition, a coherent system allows for easy extraction of signal phase[4].

The following user requirements were identified:

1. A prototype CW Stepped Frequency transceiver is to be designed.
2. The system must transmit in the frequency range: 500kHz - 5MHz.
3. The transmit power should be no more than 10dBm.
4. The system must utilise DDS, or Direct Digital Synthesis technology for the synthesisers.

[1]This Group is headed by Prof. M. R. Inggs, and is part of the Electrical Engineering Dept.
[2]Information supplied by Prof. Iain Mason.
[3]Information supplied by Prof. M. R. Inggs.
[4]Information supplied by Prof. M.R. Inggs.

5. The transmit, and receive modules need to operate in 47mm diameter boreholes to conform to drilling practice.

6. The system must be coherent.

1.2 Outline of dissertation

The dissertation consists of 7 main chapters of discussion:

1. The Introduction, which gives the background, and the outline of the dissertation.

2. A brief introduction into Cross-Borehole Tomography, and the image reconstruction techniques that are used in this process.

3. The reviewing of the physical model of the Radon Transform.

4. A simulation of the Borehole Tomographic process.

5. The final design.

6. Test analysis of the design.

7. Conclusions, and recommendations based on the findings, and investigations within the dissertation.

1.2.1 Introduction

The first chapter explains the background behind the dissertation, and gives a short, but detailed summary of each of the main chapters of the dissertation.

1.2.2 Cross-Borehole Tomography

The second chapter explains the principle behind Cross-Borehole Tomography, and looks a little deeper into the procedure involved [11, page 2]. The procedure involves placing a transmitter, and a receiver in two different boreholes, and moving them to different positions. At each position the receiver captures the phase, and the

amplitude information [11, 5, page 3]. This information is used in an inverse process which results in image reconstruction of the subsurface [2].

This chapter discusses the environmental factors that need to be considered, when designing a subsurface system [3], [5], [13]: Clay rich sediments within the borehole can absorb the radar energy making propagation through the subsurface impossible [3, page 11]. The use of low transmit frequencies are required to propagate through the subsurface [5, page 3]. The system needs to be low powered due to the explosive hazard of gases present within the subsurface. The quality of the measurements taken at the receiver are severly limited by borehole geometry [3, page 10]. The high temperatures within the borehole require some sort of cooling process for the electronic hardware [5, page 7].

The Radon Transform is defined. This transform forms the basis of all Tomography [1, page 12, (2.5)].

This chapter explains three possible image reconstruction techniques that can be used: Projection-Slice Theorem [2, page 202], Backprojection [2, page 205], and Iterative Methods [11, page 2]. The University of Sydney utilises the Iterative Methods technique when performing image reconstruction, which essentially involves solving a system of linear equations [11].

1.2.3 Physical Model of the Radon Transform

The third chapter reviews the physical model of the Radon Transform concerning bulk attenuation, and traveltime for both the continuous case, and the discrete case [1], [11], [13], [14]. This physical model gives us an understanding of the mathematical process involved. The reviewing yields an interesting result: the physical model is derived from the electric field.

This chapter shows that the electrical properties situated in the subsurface (permittivity, and conductivity) effect the amplitude, velocity, and phase of the EM wave that travels through. This is the reason that an image can be obtained. This image is a spatial distribution of the permittivity, and conductivity of the media, which is mapped by the attenuation, and the velocity of the EM wave [2, page 1].

It is also shown mathematically that the traveltime is derived from the phase, and that by utilising a stepped frequency system, the problem of phase ambiguities can be solved. Finally, this chapter reviews the discrete physical model of the Radon

Transform concerning phase, and utilising a stepped frequency approach.

1.2.4 Simulation

The fourth chapter investigates a Cross-Borehole Tomographic Imaging simulation, based on the discrete physical model of the Radon Transform covered in chapter 3. The entire process is simulated in Matlab. The phase, and the amplitude are extracted by utilising IF sampling and then IQ demodulation using an easy to implement coherent demodulation technique [50, page 8]. The image reconstruction is based on the Singular Value Decomposition technique [20].

This simulation played an important part in determining the ADC resolution, LNA gain, and the frequency step size utilised for a given medium. The ADC resolution utilised is 12 bit, because this yields a better quality of image reconstruction for both the velocity, and attenuation maps compared to an ADC with 8 bit resolution. A LNA with sufficient gain is needed in order to operate in both dry, and moist earth conditions. The frequency step size utilised needs to be 2MHz or smaller, because this yields an unambiguous path length of 50 metres or greater, while displaying high quality image reconstruction. The unambiguous path length needs to be greater than 35.355 metres, which is the greatest path length in the simulated borehole geometry.

An explanation of Tomographic resolution is also given. The Tomographic resolution is determined by the number of receive positions in the borehole, and the number of pixels utilised in the imaging region. The greater the number of receive positions, and pixels utilised, the better the quality of the reconstructed image.

The simulation compares the use of phase to the use of amplitude. An interesting result is yielded: phase is more accurate than amplitude when it comes to image reconstruction. This result can be clearly understood by looking at the error analysis involved. Once again, the benefit of utilising phase instead of amplitude allows the system to operate with a lower ADC resolution. The velocity reconstruction process became distorted when the phase error was greater than 0.4 degrees.

1.2.5 Final Design

The fifth chapter covers the final design of the system. It briefly discusses three possible architectures: heterodyne, homodyne, and RF Sampling. The heterodyne system is utilised, mainly because the homodyne, and RF Sampling architectures

have problems associated with harmonics within the frequency band of interest [16, page 18, 19, and 20]. The heterodyne system is also compact, and it is desirable to have a compact system which can be utilised in 47mm diameter boreholes in order to meet the demands of the user requirements statement[5].

The system specifications are determined by the user requirements for the dissertation, general mathematical analysis of receiver systems, the results of the Matlab simulation covered in the fourth chapter, and other simulations. The IF bandwidth is 455kHz [25]. The system will operate in the transmit frequency range of 500kHz to 5MHz, as specified by the user requirements statement[6]. The frequency step size is 455kHz in order to satisfy the unambiguous path length requirement mentioned in chapter 4, and to ensure the IF remains harmonic free[7]. The BPF, or receiver bandwidth is 21kHz, which will eliminate the effect of the harmonic $\pm$45kHz away from the IF band [25].

The master clock frequency is 58.24MHz, which is a multiple of the IF frequency, and the sampling frequency [16, page 29]. The ADC will undersample the IF signal at 202.222kHz, which results in a cost effective ADC [27]. The clock to the microcontroller is 4.608MHz, which results in zero baud rate error at 2400bps, according to the baud rate simulation.

The transmit power is 9.9dBm $\approx$10dBm, as specified by the user requirements statement. The ADC has a dynamic range of 72dB, which meets the requirements mentioned in chapter 4. The maximum LNA gain is 40dB in order to satisfy the requirement of the simulated gain mentioned in chapter 4.

The receiver dynamic range is 110.96dB. The receiver dynamic range is fairly large, but this is the ideal dynamic range, and in the real world the dynamic range is likely to be lower than 100dB[8]. The compression-free dynamic range assumes that the receiver only has a single signal at the input, and that it is a desired signal [46, page 1]. It does not take into account interfering signals that are likely to lower the overall dynamic range [46, page 1].

The entire system consumes a maximum power of 6.9W when run on $\pm$5 volts[9]. The system will operate in the temperature range of 0^oC to 70^oC [24], [26], [27], [28], [29], [32], [33], [34], [35], [37], [39], [40], [41], [42].

[5]Refer to section 1.1.
[6]Refer to section 1.1.
[7]Refer to section 5.3.2.
[8]Information supplied by RF Design Engineer, Paul Fourie, from Reutech Radar Systems.
[9]Refer to Table 5.3.

The Control Module, Transmit Module, and Receive Module PCB dimensions are 152mm x 70mm, 203mm x 25mm, and 230mm x 29mm, respectively. The Control Module is not limited by size, but the Transmit Module, and Receive Module are required to operate in the 47mm diameter boreholes, as mentioned in the user requirements statement.

The fifth chapter covers the hardware, and the software implementation. The hardware is implemented by four modules: Control Module, Transmit Module, Receive Module, and the PC Module. The software is explained in detail by the flow diagrams in Appendix C.

Finally, this chapter explains the idea behind coherency, and how to implement the system's coherent control. It is important that the reference clock to both the synthesisers be phase-locked with each other in order to establish a frequency to frequency coherent system. The synthesisers need to be reset in order to place the synthesisers in the same phase, and state [24, page 5, and 11]. The frequency update signal must be synchronised with the reference clock, sample clock, and the synthesiser system clock frequency must be a multiple of the IF frequency, as explained in section 5.5. The sampling must take place on the sample clock, as shown in Figure 5.9.

1.2.6 Design and Test Analysis

The sixth chapter involves the test analysis of the final design. It concentrates on the following areas of testing: the compression-free receiver dynamic range, transmitter power, LNA gain, BPF harmonics, and ADC harmonics. Finally, this chapter tests the overall system coherency.

The compression-free receiver dynamic range is measured to be 55.06dB, which is 55.9dB less than the ideal calculated value in section 5.3.7. There also appears to be coupling of the 58.24MHz synthesiser clock signal, and the 9.2MHz harmonic of the 4.608MHz microcontroller clock frequency onto the LNA input[10]. This is caused by the auto-routing of the boards due to time-constraints.

The transmitter power is measured to be within the user-requirements 10dBm[11] value for the entire transmit frequency range. The measured LNA gain corresponds to the programmed LNA gain. However, when the gain is set to 40dB the output

[10] Refer to section 6.2.
[11] Refer to section 1.1.

signal becomes distorted due to the above mentioned coupling.

The analysis of the BPF output, and input ADC harmonics shows that there is coupling of the above mentioned clock signals, including the 9.707MHz system clock signal. There is local oscillator feedthrough appearing. However, there is good suppression of the coupled clock signals from the IF signal at the ADC input. The 9.707MHz, 4.608MHz, 9.2MHz, and 58.24MHz clock signals are 45.5dB, 49.5dB, 44.5dB, and 41.5dB lower than the required IF signal, respectively. The local oscillator feedthrough is 28dB lower that the required IF signal. The oscilloscope shows that the ADC input IF signal appears to be fairly clean for the entire transmit frequency range.

Finally, the frequency to frequency coherency test for the entire transmit frequency range showed that the system is indeed frequency to frequency coherent[12]. The transmit frequencies, 1.465MHz, 2.375MHz, 3.285MHz, 4.65MHz, and 5.105MHz, all have a change in phase error of less than, or equal to 0.4 degrees, and are therefore, within the desired accuracy in order to reconstruct a high quality velocity map image[13] . However, the transmit frequencies, 555kHz, 1.01MHz, 1.92MHz, 2.83MHz, and 3.74MHz, will have a change in phase error that will not always be less than or equal to 0.4 degrees, and hence, distortion of the reconstructed velocity map image can occur.

The utilisation of a 12 bit ADC should yield a maximum phase error of 0.027 degrees, as mentioned in section 4.7.2. However, the actual phase error is greater than this. This is probably due to inefficient PCB routing, and supply bypassing around the ADC, and the rest of the system[14] [27, page 15].

1.2.7 Conclusions and Recommendations

The final, and seventh chapter gives the conclusions, and the recommendations based on the findings, and investigations within the dissertation. The following main conclusions are drawn:

- The phase yields a better quality of image reconstruction than amplitude, and hence a coherent system is a good choice. The use of phase allows for a lower system ADC Resolution, as proven in section 4.7.2.

[12]Refer to section 6.6.
[13]Refer to section 4.7.2.
[14]Refer to section 6.2.

- A heterodyne system is the system of choice, because harmonics are factored out of the equation due to the BPF bandwidth, and the choice of transmit frequencies [16, page 18, 19, and 20].

- No error checking is performed on the protocol used in the software, as mentioned in section 5.4.1. Therefore, error in data transmission can occur.

- The system's compression-free dynamic range, LNA gain, BPF output, and ADC input are all being effected by the undesirable coupling of the 58.24MHz synthesiser clock signal, the 9.707MHz system clock signal, and the 4.608MHz crystal frequency for the microcontroller, with its 9.2MHz harmonic[15]. The BPF output, and the ADC input are also experiencing local oscillator feedthrough, as mentioned in section 6.5. The local oscillator is being fed through, because the output signal of the mixer is relatively small ($\leq -6dBm$) in amplitude, and therefore, the BPF (optimum input $\geq 0dBm$) has no effect [25, page 6], [36, page 56].

- The system is frequency to frequency coherent for the entire transmit frequency range, which satisfies the main aim of this dissertation[16].

- Finally, the system satisfies all the requirements of the user requirements statement covered in section 1.1.

The following main recommendations can be made:

1. The software protocol must incorporate error checking in the future to guarantee the arrival of the data message. This will prevent timing problems from occuring if a faster PC is utilised. A suggested protocol to use is TCP, or transmission control protocol [49, page 78].

2. The next prototype must utilise proper RF PCB routing methods, and must incorporate a power, and ground plane in order to eliminate the coupling of the above mentioned clock signals [47, page 455]. This will help to lower the noise floor, and therefore, improve the system compression-free dynamic range[17]. The introduction of a ground plane helps to eliminate, or reduce any potential difference in the grounds between the ADC, and the rest of the analogue circuitry, which will appear as an error voltage in series with the

[15] Refer to sections 6.2, 6.4, and 6.5.
[16] Refer to section 6.6.
[17] Refer to equation 5.1.

ADC analog input signal [27, page 15]. This will improve the overall change in phase accuracy.

3. The IF amplifier must be placed after the mixer, and the BPF must be placed after the the IF amplifier. This will ensure that the BPF attenuates the local oscillator feedthrough effectively [25, page 6].

4. The current system must utilise coherent integration in order to improve the change in phase accuracy, so that the error is less than or equal to 0.4 degrees[18] [18, page 144]. This will ensure that the velocity map image can be reconstructed without distortion occuring.

5. Finally, a fully-functional system that can be used in the field should be designed. This involves designing the transmit, and receive antenna. Special emphasis must be placed on the fibre optics involved, because the cables can become snagged, and break loose in the borehole.[19]

[18] Refer to section 4.7.2, and 6.6.
[19] Information supplied by Prof. Iain Mason.

Chapter 2

Cross-Borehole Tomography

2.1 Introduction

This chapter, briefly, discusses the Cross-Borehole Electromagnetic Imaging technique. The technique's advantages, uses, and the implementation are mainly discussed.

The environmental factors that effect the propagation of the EM waves are looked at in detail. A Tomographic image is defined.

Finally, the Radon Transform, which forms the basis of all tomography is defined, and three image reconstruction techniques are investigated: Projection-Slice Theorem, Backprojection, and Iterative Methods.

2.2 Cross-Borehole Electromagnetic Imaging

There are many techniques which can be used to implement Borehole Tomography. For example, there is Electrical Resistance Tomography, which images the resistivity of the subsurface image. Electrical Resistance Tomography has an advantage over electromagnetic imaging in that fewer boreholes are required [4]. This dissertation will use the technique called Cross-Borehole Electromagnetic Imaging [11, page 2].

This process produces an image of the attenuation or the velocity of the electromagnetic waves sent through the subsurface [11, page 1]. This technique results in fast performance, large area coverage, and its implementation is inexpensive [7],

[10]. This method has been widely used for non-invasive detection of underground metallic and chemical waste forms, such as chromium [10].

The cross-borehole process can be seen in Figure 2.1. The transmitter is placed in position P1 while the receiver is moved from P1 to Pn. The transmitter is then moved to P2 and the receiver is moved from P1 to Pn again. This process is repeated until the transmitter has covered every position. At each position, the receiver captures the phase (traveltime) or amplitude information [11], [5, page 3]. The information is used in an inverse process which results in target reconstruction [2].

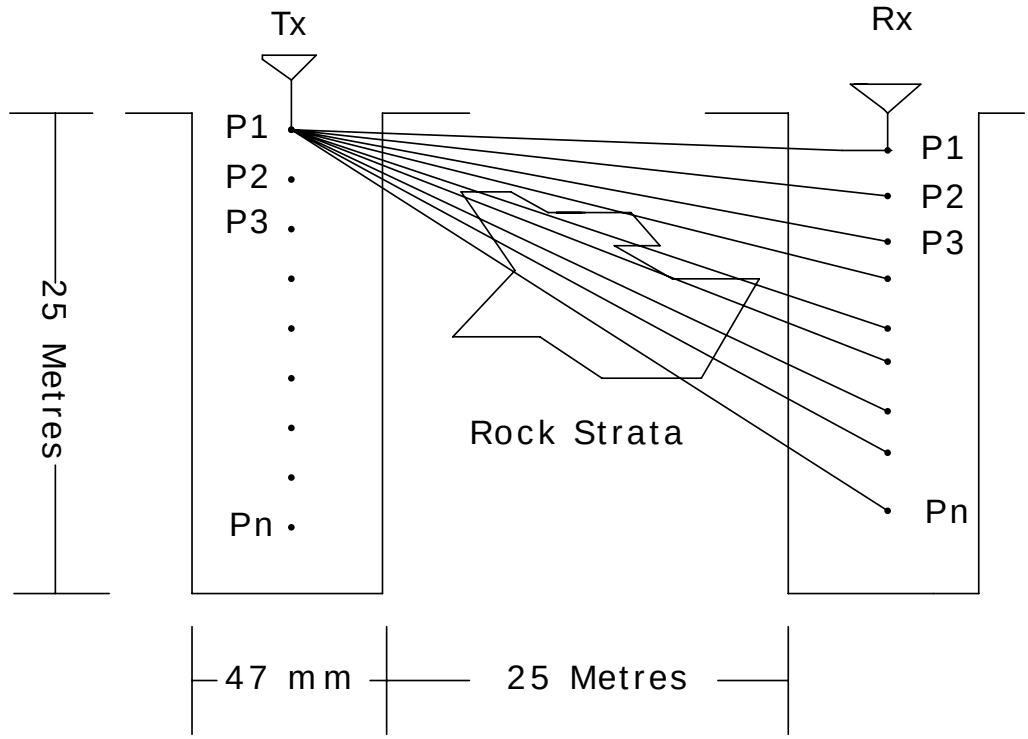

Figure 2.1: The Cross-Borehole Technique with Dimensions

2.3 Environmental Factors

Tomographic images are mappings of the permittivity and conductivity of the target media, which are related to the attenuation and the velocity of the EM wave [2, page 1]. The following properties of the media effect the propagation of the EM waves and gives important information towards the system design:

1. The dielectric constant or relative permittivity of the subsurface material, for

example, water has a higher dielectric constant than air. The imaginary part of the dielectric constant or the loss tangent will effect the attenuation of the wave and the real part of the permittivity will effect the velocity of the wave [13, page 30]. The presence of small amounts of clay-rich sediments in drilling fluids can have the effect of absorbing all the radar energy, and hence, propagation through the subsurface would be impossible [3, page 11].

2. Low frequencies need to be used, because the propagation distance through-the-earth for high frequencies is severly limited [5, page 3]. Operating at high frequencies means that the attenuation depends on the conductivity as well as the permittivity of the medium, but at lower frequencies attenuation is independent of permittivity and dependent on conductivity which accounts for ionic losses/conductivity losses [5, page 3].

3. The system needs to be low-powered, because of the possible explosive hazard of gases situated in the subsurface[1]. Therefore, an issue of safety needs to be considered.

4. The borehole results obtained are severly limited by the hole geometry. The deeper the borehole the greater the ray coverage, and hence, the better the quality of the radar measurements [3, page 10].

5. Hardware enclosures - electronics will be placed in the borehole which means that the components must be able to withstand the extreme temperatures and the moisture in the boreholes. For example, watertight bakelite containers filled with transformer oil can be used to dissipate the heat so that the electronics can survive under extreme temperature conditions [5, page 7].

2.4 Image Reconstruction Techniques

In order to obtain an image of the attenuation or velocity of the EM wave through the medium requires first obtaining various profiles, at different angles, of the image medium. Radar imaging is very similar to tomographic imaging except that instead of considering profiles one considers range [2, page 201]. There is a well defined transform which forms the basis of the process tomography. This transform is called

[1]Information supplied by Dr. Alan Langman.

the Radon Transform and can be found in Dean's book [1, page 12, (2.5)].

$$P(\rho, \phi) = \int_L \mu(x, y) ds \tag{2.1}$$

Equation 2.1 represents the Radon Transform and is nothing more than the line integral of the spatial distribution of the physical property that is used for imaging, $\mu(x, y)$, which gives rise to the various profiles, $P(\rho, \phi)$, at different angles, ϕ, and lengths, ρ.

The hardware will obtain the profiles at various different angles. It is important to note that in cross-borehole tomography the projection or profile angles are limited because of the use of vertical boreholes [5, page 3]. The profiles are obtained by either using the phase (traveltime) or amplitude information at the receiver [11, page 2]. Many projections need to be obtained in order to get a fairly complete image of the spatial distribution of the physical property (wave attenuation or velocity) in question.

The image can be obtained by using software that contains an image reconstruction technique. The software at the University of Sydney, uses the Iterative Methods technique [11]. There are quite a few methods that can be used, but the methods that will be dealt with in this dissertation, briefly, are the following:

- Projection-Slice Theorem or Fourier Reconstruction Technique
- Backprojection
- Iterative Methods

2.4.1 Projection-Slice Theorem

This technique relates the one-dimensional Fourier transform of a projection to a central section or slice of the two-dimensional Fourier transform of the imaging distribution [2, page 202]. This is a very important result, because it means that if a large number of projections can be obtained then the result is a very good approximation to the two-dimensional Fourier transform of the imaging property using only one-dimensional transforms of the projections. The whole reconstruction process can be summarised as follows [2, page 202]:

1. Fourier transfom each projection.

2. Interpolate to fill in missing data due to a finite number of projections.

3. Perform the two-dimensional Fourier transform of the results.

2.4.2 Backprojection

This technique obtains an estimate of the image by using the backprojections of the projections or profiles. It is able to obtain an estimate because it sums up all the backprojections from all possible angles. The process may be summarised as follows [2, page 205]:

1. Given a projection $P(\rho, \phi)$ for a specific angle, the backprojection process assigns the value of the projection to all points in the imaging or x,y space which corresponds to a given ρ.

2. The summation image is formed by the superposition of backprojections from all possible angles.

The more profiles or projections obtained the better the quality of the image will be. It turns out that the image formed by this technique is often blurred and hence some sort of filtering process must be used for deblurring.

2.4.3 Iterative Methods

Iterative methods involve solving a system of linear equations. It can be summarised as follows [11, page 2]:

1. The image region is divided into a grid of cells through which the individual electromagnetic waves will pass.

2. Every cell is given a constant attenuation value or velocity value (α), each wave has a measured attenuation value at the receiver or phase (traveltime) and a certain length through each cell.

3. Therefore, every wave forms an equation in the unknown α.

4. The set of equations are solved by iterative methods to determine the unknowns.

This method assumes straight line propagation [11, page 2]. This means multipath effects are ignored. In order to deal with the diffraction of the wave in the subsurface a process called Diffraction Tomography could also be employed [6].

2.5 Conclusion

In conclusion, the Cross-Borehole Electromagnetic Imaging technique is fast to implement, and relatively inexpensive.

The environmental factors give important information towards the final system design. The system requires a low transmit frequency range in order to propagate through the earth, and needs to be low-powered, because of the possible explosive hazard of gases present within the subsurface. The components must be able to withstand the extreme temperatures, and the moisture in the boreholes.

Finally, hardware needs to be designed that can capture the phase (traveltime), and amplitude information profiles at the receiver. There are quite a few methods that can be used to implement image reconstruction, but this dissertation will utilise the Iterative Methods technique.

Chapter 3

Physical Model of the Radon Transform

3.1 Introduction

This chapter shows that the physical model of the Radon Transform can be derived by using the E-field of the EM wave transmitted underground, instead of the signal itself. This chapter shows that the electrical properties situated in the subsurface (the permittivity and conductivity) effect the following of the E-field:

- Amplitude
- Velocity
- Phase

It is due to this effect that an image of the subsurface can be obtained. In Section 3.2, the physical model of the Radon Transform for the continuous case is reviewed and in Section 3.3, the same model is reviewed for the discrete case. Finally, the discrete physical model of the Radon Transform concerning phase, and utilising a stepped frequency approach is examined.

3.2 Continuous Case

The tomographic image (in this case) is a spatial distribution of the permittivity and conductivity of the media, which is mapped by the attenuation and the velocity of the EM wave [2, page 1]. The Radon Transform is given by Equation 3.1 [11, page 1] for the continuous case.

$$d_i = \int_L p(l)dl \tag{3.1}$$

In Equation 3.1 , $p(l)$ represents the attenuation or the velocity of the EM wave and d_i represents the amplitude or traveltime for the i_{th} raypath. The Physical Model of the Radon Transform can be derived by looking at the E-field of the EM wave. The E-field propagating through a general lossy medium[1] is given by Equation 3.2 [13, page 29].

$$E(z) = E_o \cdot e^{-\alpha z} \cdot e^{-j\beta z} \tag{3.2}$$

In Equation 3.2, α is the attenuation constant, β is is the phase constant, E_o is the initial E-field constant and z is the direction of the propagation. The E-field propagation can be seen in Figure 3.3. The propagation takes place over the path length (p to q) and hence, straight line propagation is assumed. If the co-ordinate system of Figure 3.3 is used and the Z-axis is assumed to be perpendicular to the X and Y axes, then Equation 3.2 can be expressed as follows:

$$E_{pq}(X_1, Y_1) = E_{pq}(0, Y_0) \cdot e^{-\int_L \alpha(X,Y)dS_{pq}} \cdot e^{-j\int_L \beta(X,Y)dS_{pq}} \tag{3.3}$$

Equation 3.3 represents the E-field as it propagates along the length of the path ($L = pq$) from the transmitter, $E_{pq}(0, Y_0)$, to the receiver, $E_{pq}(X_1, Y_1)$, where $p = 0$ to P and $q = 0$ to Q[2]. P represents the number of transmit positions and Q represents the number of receive positions. Equation 3.3, as it stands, is not linear and it can be linearized by taking the natural logs of both sides to obtain:

$$-ln\left[\frac{E_{pq}(X_1, Y_1)}{E_{pq}(0, Y_o)}\right] = \int_L \left[\alpha(X,Y) + j\beta(X,Y)\right] dS_{pq} \tag{3.4}$$

[1] See Figure 3.1 for definition

[2] Refer to Figure 3.3.

The E-field has the units $\left[\frac{V}{m}\right]$. Therefore, the LHS of Equation 3.4 represents the voltage amplitude of the signals. The amplitude of the signals is dependent on the attenuation constant rather than the phase constant and so by taking the real part of Equation 3.4 and replacing the E-field with the voltage amplitudes renders the following equation:

$$-ln\left[\frac{A_{pq}(X_1,Y_1)}{A_{pq}(0,Y_o)}\right] = \int_L \alpha(X,Y)dS_{pq} \tag{3.5}$$

Equation 3.5 represents the Radon Transform in terms of the amplitude and the attenuation constant[3]. The phase constant is related to the propagation velocity in the following way [13, page 30]:

$$V(X,Y) = \frac{\omega}{\beta(X,Y)} \tag{3.6}$$

In Equation 3.6 , $V(X,Y)$ represents the propagation velocity and $\omega = 2\pi f$ (f represents the transmit frequency). The Radon Transform in terms of the traveltime and the propagation velocity is as follows [1, page 23]:

$$T_{pq} = \int_L \frac{1}{V(X,Y)}dS_{pq} \tag{3.7}$$

The Radon Transform clearly shows that the imaging data (velocity or attenuation) can be related to the information at the receiver (traveltime or amplitude). This means that if the phase measurement is utilized it can be related to the imaging data (phase constant).

In order to obtain the physical model of the Radon Transform a relationship has to be obtained between the imaging data and the electrical properties of the media[4]. The following equations represent this relationship for general lossy media [13, page 30]:

$$\alpha(X,Y) = \omega \cdot \sqrt{\mu(X,Y)\cdot\frac{\epsilon'(X,Y)}{2}\cdot\left[\sqrt{1+\left(\frac{\epsilon''(X,Y)}{\epsilon'(X,Y)}\right)^2}-1\right]} \tag{3.8}$$

[3]See Equation 3.1

[4]See Figure 3.2 for definition

$$V(X,Y) = \frac{1}{\sqrt{\mu(X,Y) \cdot \frac{\epsilon'(X,Y)}{2} \cdot \left[\sqrt{1 + \left(\frac{\epsilon''(X,Y)}{\epsilon'(X,Y)}\right)^2} + 1\right]}} \tag{3.9}$$

In Equation 3.8 and Equation 3.9, $\epsilon'(X,Y)$ represents the real part of the permittivity of the media, $\epsilon''(X,Y)$ represents the imaginary part of the permittivity and $\mu(X,Y)$ represents the permeability of the media.

The following equations represent the relationship for low-loss media ($\mu(X,Y) = \mu_o$ and loss tangent $= \left(\frac{\epsilon''(X,Y)}{\epsilon'(X,Y)}\right)^2 = \left(\frac{\sigma(X,Y)}{\omega \cdot \epsilon'(X,Y)}\right)^2 \ll 1$, where $\sigma(X,Y)$ represents the conductivity of the media) [13, page 31]:

$$\alpha(X,Y) \approx (188.5).\frac{\sigma(X,Y)}{\sqrt{\epsilon_r(X,Y)}} \tag{3.10}$$

$$V(X,Y) \approx \frac{c}{\sqrt{\epsilon_r(X,Y)}} \tag{3.11}$$

In Equation 3.10 and Equation 3.11, $\epsilon_r(X,Y)$ represents the relative permittivity of the medium and c represents the speed of the electromagnetic wave in free space. The physical model for the Radon Transform (continuous case) has now been derived and now a discrete version (for our purposes) may be obtained from the continuous case.

3.3 Discrete Case

The discrete version of the Radon Transform is given by Equation [11, page 2]:

$$d_i = \sum_{j=1}^{M} p_j \cdot l_{ij} (i = 1.....N) \tag{3.12}$$

In Equation 3.12, d_i represents the amplitude or traveltime for the i_{th} raypath, p_j represents the attenuation or the velocity for pixel j, l_{ij} is the length of the i_{th} ray that passes the j_{th} pixel, M represents the total number of pixels and N represents the total number of rays. This discrete Radon Transform is derived by using the co-ordinate system of Figure 3.4 and transforming Equation 3.3 of Section 3.2 in to

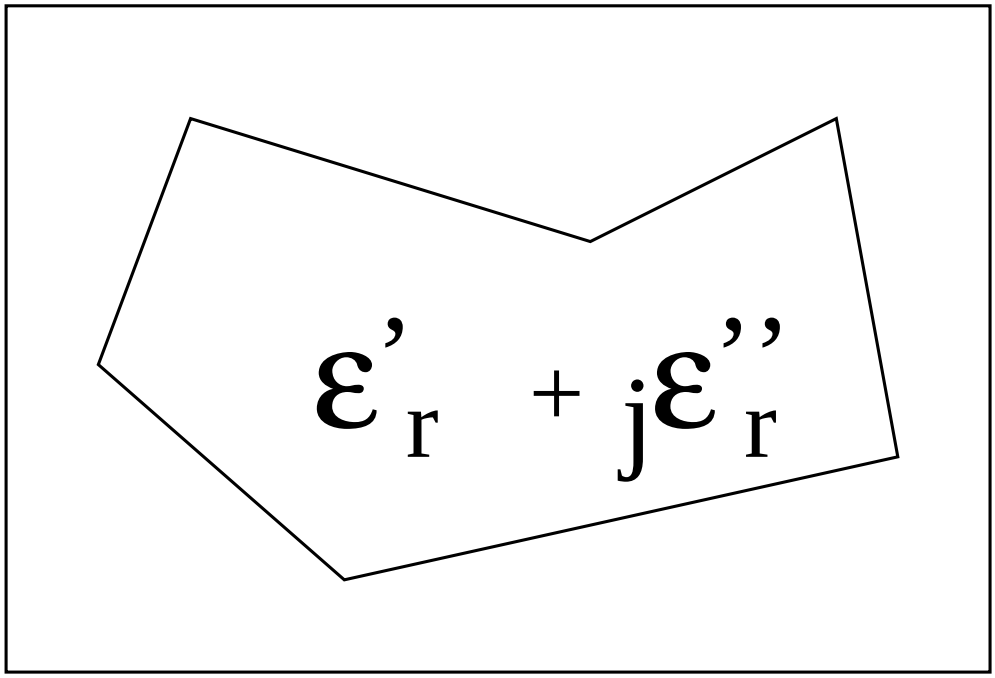

Figure 3.1: Definition of Medium

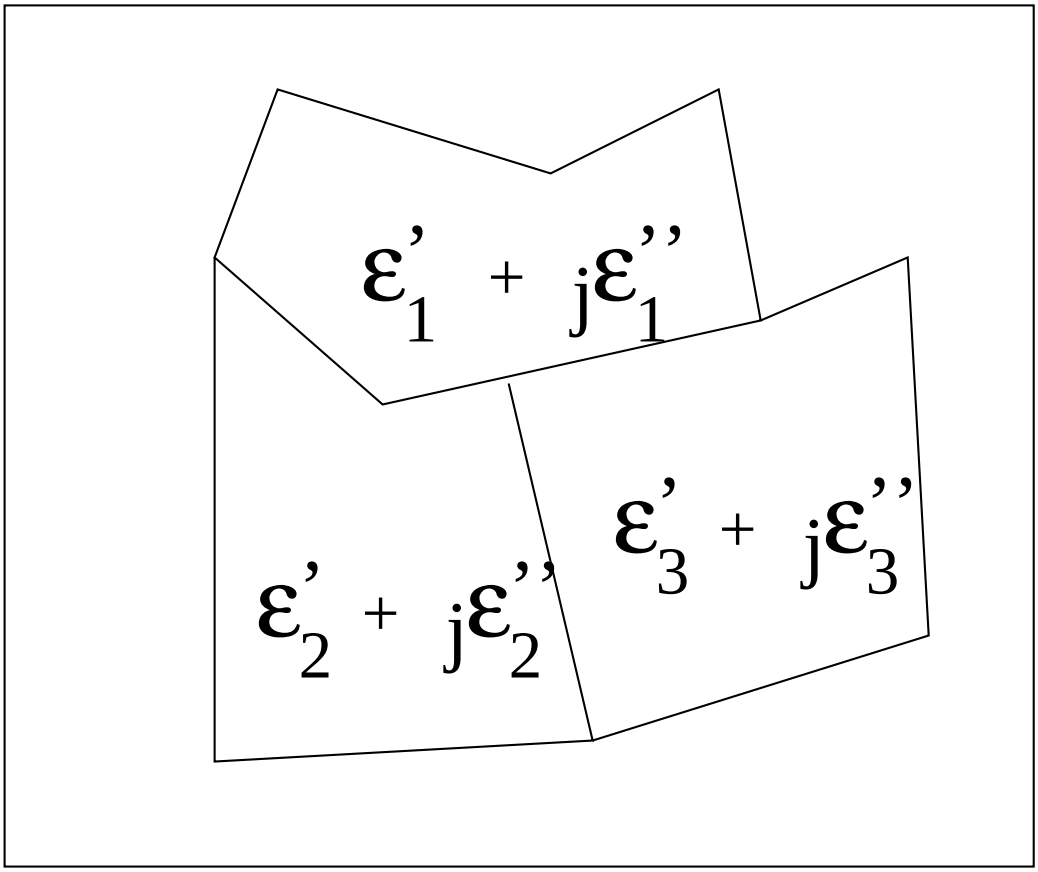

Figure 3.2: Definition of Media

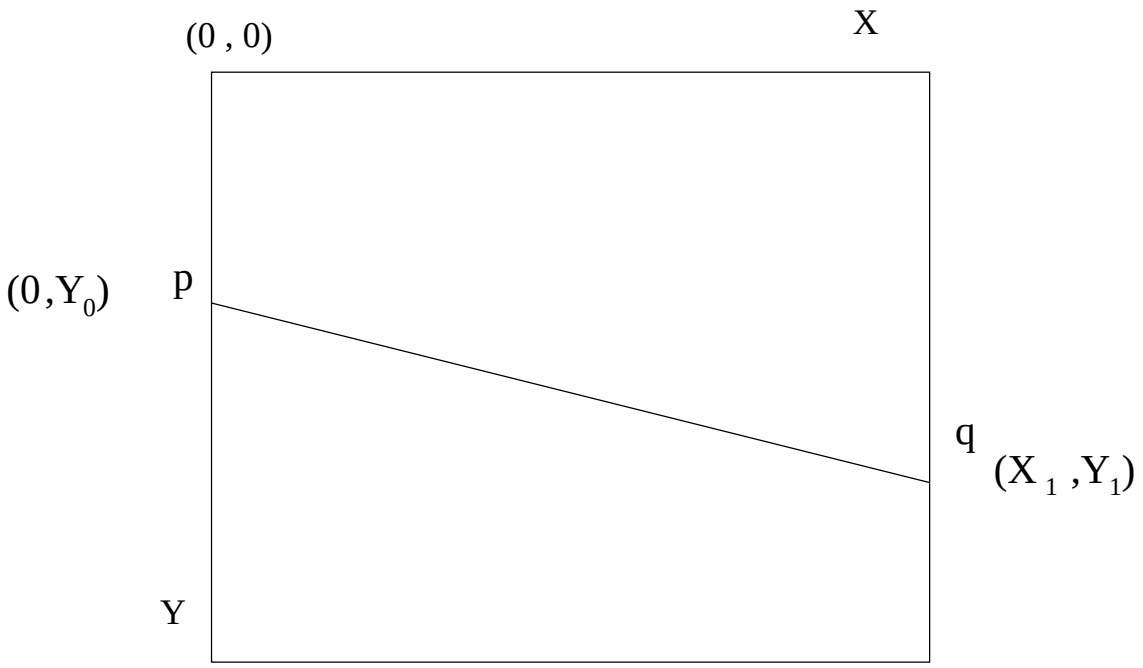

Figure 3.3: Continuous Propagation of the E-Field

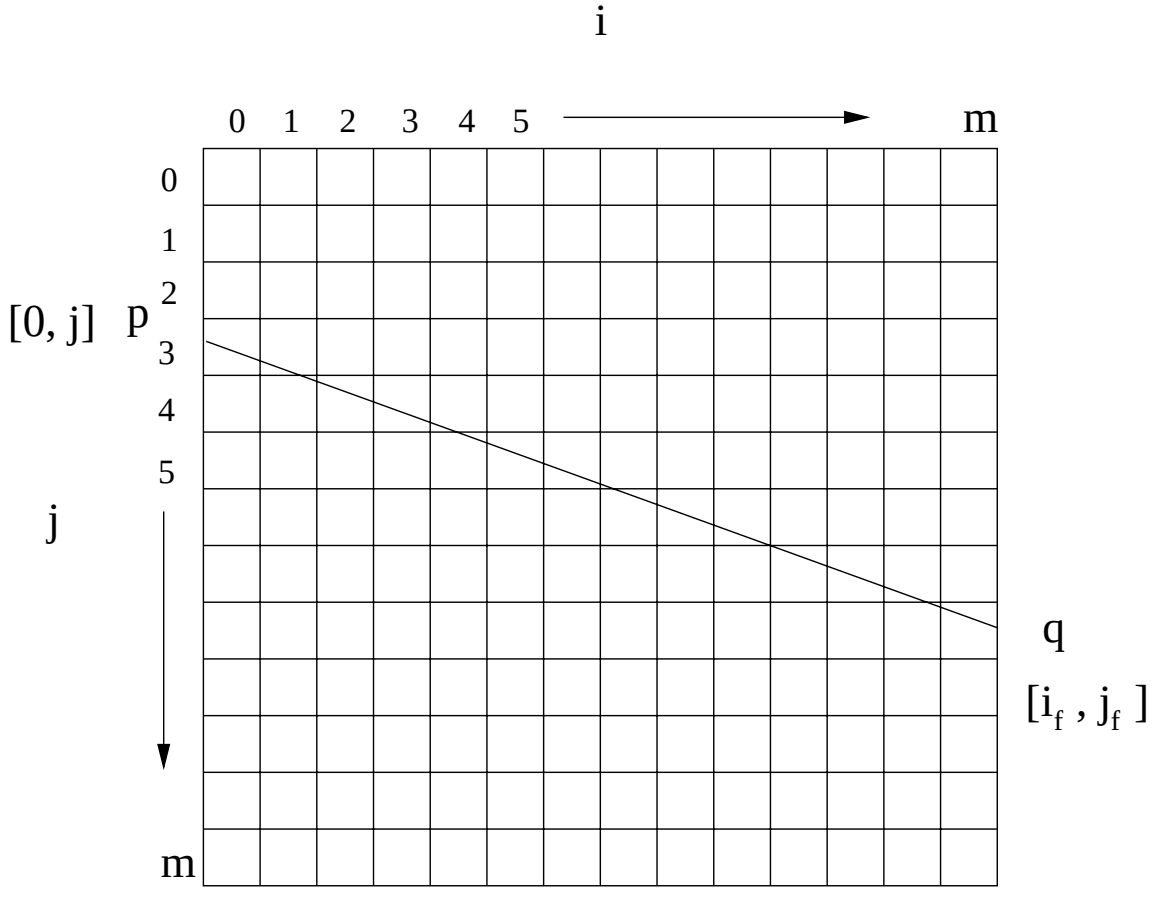

Figure 3.4: Discrete Propagation of the E-Field

its discrete form by using definition 14.6 [14, page 856]:

$$E_{pq}[i_f, j_f] = E_{pq}[0, j] \cdot e^{-\sum_{i=0}^{m} \sum_{j=0}^{m} \alpha[i,j].\triangle S[i,j]_{pq}} \cdot e^{-j \sum_{i=0}^{m} \sum_{j=0}^{m} \beta[i,j].\triangle S[i,j]_{pq}} \quad (3.13)$$

In Equation 3.13, $\alpha[i,j]$ represents the attenuation constant for pixel $[i,j]$, $\beta[i,j]$ represents the phase constant for pixel $[i,j]$, $\triangle S[i,j]_{pq}$ represents the length of the ray pq through pixel $[i,j]$ (assumes that the limit of the maximum length $\rightarrow 0$ from definition 14.6 [14, page 856]) and m represents the number of i columns and j rows (the rows and columns are assumed to be the same for simplification). Taking the natural logs of both sides of Equation 3.13 and using the same assumptions for the continuous case renders the following equation:

$$-ln\left[\frac{A_{pq}[if, jf]}{A_{pq}[0, j]}\right] = \sum_{i=0}^{m} \sum_{j=0}^{m} \alpha[i,j] \cdot \triangle S[i,j]_{pq} \quad (3.14)$$

Equation 3.14 represents the discrete Radon Transform in terms of the amplitude and attenuation constants[5]. The discrete Radon Transform concerning traveltime and propagation velocity may be obtained by converting Equation 3.7 in to its discrete form by using definition 14.6 [14, page 856] and using the co-ordinate system of Figure 3.4:

$$T_{pq} = \sum_{i=0}^{m} \sum_{j=0}^{m} \frac{1}{V[i,j]} \cdot \triangle S[i,j]_{pq} \quad (3.15)$$

The discrete physical model is obtained in the same manner as the continuous case and so converting Equations 3.8, 3.9, 3.10 and 3.11 in to the discrete case renders the following equations for general lossy media and low-loss media:

$$\alpha[i,j] = \omega \cdot \sqrt{\mu[i,j] \cdot \frac{\epsilon'[i,j]}{2} \cdot \left[\sqrt{1 + \left(\frac{\epsilon''[i,j]}{\epsilon'[i,j]}\right)^2} - 1\right]} \quad (3.16)$$

$$V[i,j] = \frac{1}{\sqrt{\mu[i,j] \cdot \frac{\epsilon'[i,j]}{2} \cdot \left[\sqrt{1 + \left(\frac{\epsilon''[i,j]}{\epsilon'[i,j]}\right)^2} + 1\right]}} \quad (3.17)$$

[5]See Equation 3.12

$$\alpha[i,j] \approx (188.5) \cdot \frac{\sigma[i,j]}{\sqrt{\epsilon_r[i,j]}} \tag{3.18}$$

$$V[i,j] \approx \frac{c}{\sqrt{\epsilon_r[i,j]}} \tag{3.19}$$

Therefore, the physical model of the Radon Transform for the discrete case has been derived. It should be noted that at this point in time the model does not take in to account the stepped frequency capability or the phase as a measurement.

Equation 3.15 concerns itself with the traveltime, but the system under design will capture phase measurements, and extract the traveltime from the captured phase measurements. In fact, it turns out that by measuring the phase directly, and then extracting the traveltime is much more efficient than measuring the traveltime directly[6]. It is important to note that the measured phase signal can only take on values in a 2π range, while the true phase signal can take on any value, and hence, create phase ambiguities. This is known as phase wrapping [51]. The phase will need to be unwrapped in order to extract the true traveltime, as discussed below.

This implies that the change in phase must be related to the traveltime. This is proved by the following equations [17, page 104]:

$$\beta = k = \frac{2\pi}{\lambda} \tag{3.20}$$

$$\lambda = \frac{\nu}{f} \tag{3.21}$$

$$L = \nu \cdot T_{pq} \tag{3.22}$$

In equation 3.20, β represents the phase constant, or the angular wave number of the travelling waveform, and λ represents the wavelength of the travelling waveform. In equation 3.21, v represents the velocity of the travelling wave, and f represents the frequency of the travelling wave. In equation 3.22, L represents the total distance the travelling wave has travelled in metres, and T_{pq} represents the traveltime of the travelling wave along ray path pq[7] . The units of β are $\frac{\phi}{m}$, where ϕ represents the

[6]Information supplied by Dr. Alan Langman

[7]See equation 3.15

phase (rads) of the travelling wavefom, and m represents the length in metres. In order to derive the $\triangle\phi$ (change in phase), equation 3.20 will have to be multiplied by equation 3.22. The result is the following equation:

$$\triangle\phi = 2\pi \cdot f \cdot T_{pq} = \omega \cdot T_{pq} \tag{3.23}$$

Equation 3.23 clearly shows that the traveltime is related to the change in phase by a factor of ω, which represents the angular frequency. Equation 3.23 at this time does not take in to account unambiguous phase, because it is phase wrapped as mentioned above. This means that equation 3.23 is only valid if the total change in phase is less than or equal to 2π [18, page 84]. This implies that the transmitter needs to transmit at a frequency that has a wavelength greater than the distance between the two boreholes to ensure that the change in phase is less than 2π. The ambiguous phase problem can be solved by using a stepped frequency approach [18, page 84]. In order for the unambiguous phase to be taken into account, a new factor needs to be added to equation 3.23 to yield the following final equations:

$$\triangle\phi_x + 2\pi n_x = 2\pi \cdot f_x \cdot T_{pq} \, (n_x = 0, 1, 2...\infty;\, x = 1, 2...X) \tag{3.24}$$

$$T_{pq} = \frac{\triangle\phi_x + 2\pi n_x}{2\pi \cdot f_x} \, (n_x = 0, 1, 2...\infty;\, x = 1, 2...X) \tag{3.25}$$

In equation 3.24, and 3.25, factor $2\pi n_x$ accounts for the fact that multiple cycles or phase shifts of 2π radians have resulted where n_x represents the number of complete transmit cycles that have occurred when sampling begins at the receiver. The factor f_x accounts for a stepped frequency situation, and X represents the total number of transmit frequencies.

The discrete physical model of the Radon Transform concerning phase may be obtained by substituting Equation 3.15 into equation 3.24 or 3.25 and using the coordinate system of Figure 3.4. Equation 3.25 cannot be solved without using a stepped frequency approach, since if only one transmit frequency is used then there would be two unknowns (T_{pq} and n_x), and in order to solve the two unknowns at least two equations are needed [19]. However, if we use two or more transmit frequencies travelling along the same ray path pq the traveltime must be the same for both or more frequencies, since traveltime is dependent on the velocity of the

travelling wave, and the travel distance of the wave[8] . The velocity is in turn dependent on the permittivity, and this will not change along the same ray path pq [9]. The length along the ray path will stay the same. Hence, the fact that the traveltime is the same for two or more transmit frequencies means that equation 3.25 can be equated with itself to yield the following equation:

$$\frac{\triangle\phi_1 + 2\pi n_1}{2\pi \cdot f_1} = \frac{\triangle\phi_2 + 2\pi n_2}{2\pi \cdot f_2} = \frac{\triangle\phi_x + 2\pi n_x}{2\pi \cdot f_x} \tag{3.26}$$

$$(n_x = 0, 1, 2...\infty;\ x = 1, 2...X)$$

The only unknowns now are n_1 and n_2, $\triangle\phi_1$ and $\triangle\phi_2$ are captured by the receiver. It is just a question of substituting integer values for these two unknowns until the equations are equivalent. Once this occurs, then the traveltime (T_{pq}) is known, and hence, the phase is correctly unwrapped.

3.4 Conclusion

In conclusion, the physical model of the Radon Transform is derived from the electric field. The Radon Transform clearly shows that the velocity and the attenuation of the EM wave propagating through the image medium can be related to the phase (traveltime) and bulk amplitude at the receiver, respectively.

The measured phase at the receiver is phase wrapped, and hence, phase ambiguities can occur. This phase wrapping places limitations on the transmit frequency range. A stepped frequency system allows for proper phase unwrapping, and hence, the true traveltime can be extracted from the measured phase without limiting the transmit frequency range.

[8] See equation 3.22
[9] See equation 3.17, and 3.19

Chapter 4

Simulation

4.1 Introduction

The simulation performs the entire Cross-Borehole EM Imaging process[1]. The Tomographic simulation utilises the discrete equations that are reviewed in Chapter 3, especially the traveltime physical model, and the attenuation physical model of the Radon Transform.

This chapter covers the following:

- Explains the simulation procedure by means of a flow diagram located in Appendix B.
- Discusses, and uses the simulation to determine the ADC resolution, LNA gain, and the frequency step size.
- The concept of Tomographic resolution is introduced, and examined.
- Finally, the simulation compares the use of phase to the use of amplitude.

4.2 Tomographic Simulation

The simulation is written in Matlab, and the source code may be found on the Borehole Tomography CD[2]. This chapter will only discuss the main findings during

[1] Refer to Chapter 2.
[2] File location on CD: D:\simulation\Tomo*.m

the simulation process. If a more detailed understanding is needed please refer to the source code for more information.

The simulation procedure is illustrated by a flow diagram in Figure B.1, which may be found in Appendix B. The first stage involves plotting the transmit, and receive positions defined by the user input. The second stage involves plotting the pixel area, and the ray paths defined by the user input. The user input is listed with typical values in Table 4.1. A typical borehole geometry generated with the user input values of Table 4.1 is shown in Figure 4.1. The left hand y-axis represents the Tx Position, and the right hand y-axis represents the Rx Position. The length, and width are set at 25 metres (adjustable), because the final system will eventually be tested with this geometry[3].

Table 4.1: User Input Typical Values

USER INPUT	**TYPICAL VALUES**
Tx Positions	8
Rx Positions	8
Pixel Size (row)	8
Pixel Size (cols)	8
Tx Phase (degrees)	0
Minimum Tx Frequency (Hz)	500000
Maximum Tx Frequency (Hz)	5000000
Tx Voltage (V)	1
Full-Scale Value of ADC (V)	2
Quantization Noise of ADC (V)	1e-3
ADC Input Voltage (V)	2
Frequency Step Size (Hz)	$\leq$2000000

The third, and fourth stages involve plotting the velocity, and attenuation matrices/maps. The simulation assumes that the media is homogenous, low-loss, and non-magnetic in nature. Therefore, equation 3.18, and 3.19 from Chapter 3 were used to calculate the attenuation constants, and the velocity constants, respectively. The conductivity, $\sigma[i,j]$, was set at 1e-3 $(\Omega \cdot m)^{-1}$,which represents the conductivity value for dry earth [15, page 283]. The relative permittivity, $\epsilon_r[i,j]$, ranges from 4 to 9, where 9 represents the value for sand [15, page 283]. The simulated attenuation map can be seen on the left hand side of Figure 4.2, and the simulated velocity map can be seen on the left hand side of Figure 4.3. The velocity and attenuation simulated, and reconstructed maps both have shading value scales located on the

[3]Information Supplied by Prof. Iain Mason.

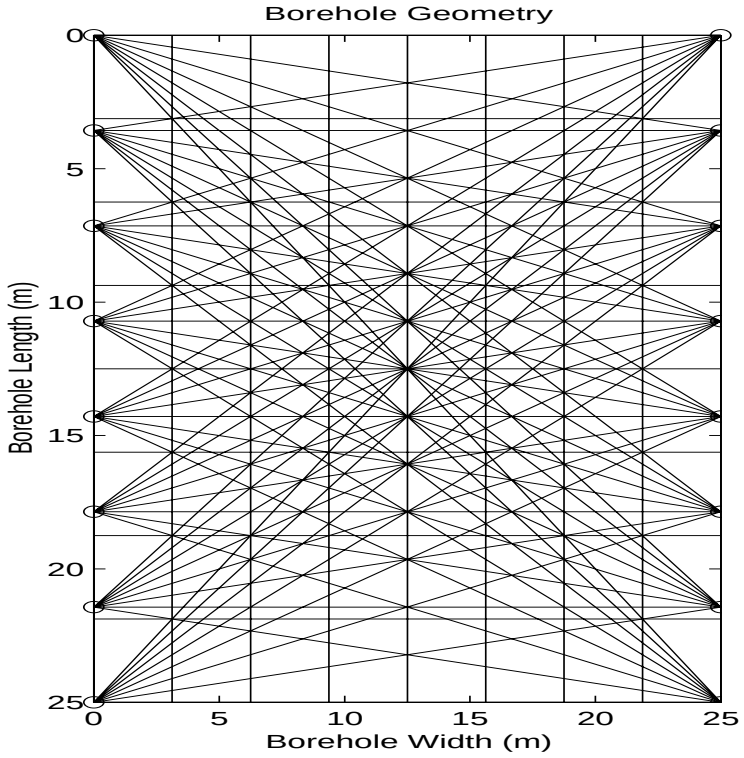

Figure 4.1: A Typical Borehole Geometry

right of each map. The attenuation map scale is in Nepers per a metre $\left[\frac{Np}{m}\right]$, and the velocity map scale is in metres per a second $\left[\frac{m}{s}\right]$.

The fifth stage involves calculating the ray intersection point with the pixels, and hence the ray lengths for each pixel. The sixth stage calculates the overall change in phase, and the bulk attenuation for each ray path length, from the Tx to Rx position. These resulting values will eventually be sampled in the IF sampling stage.

The seventh stage calculates the expected voltage return, and the required LNA gain. The eighth stage determines the ADC resolution, and adds the quantization noise specified by the user input to the ADC signal. The ninth stage performs the IF sampling algorithm [16, page 33, and 34]. The tenth stage extracts the I, and Q samples to determine the phase, and the amplitude. It also extracts the traveltime from the phase.

The eleventh stage reconstructs the simulated velocity, and attenuation map from the extracted traveltime, and amplitude values, respectively, using the Singular Value Decomposition (SVD) technique [20, page 61, and 62]. The twelfth stage performs LSQ error calculations on the phase, and on the SVD technique for both the reconstructed attenuation, and the velocity simulated maps. The error is displayed

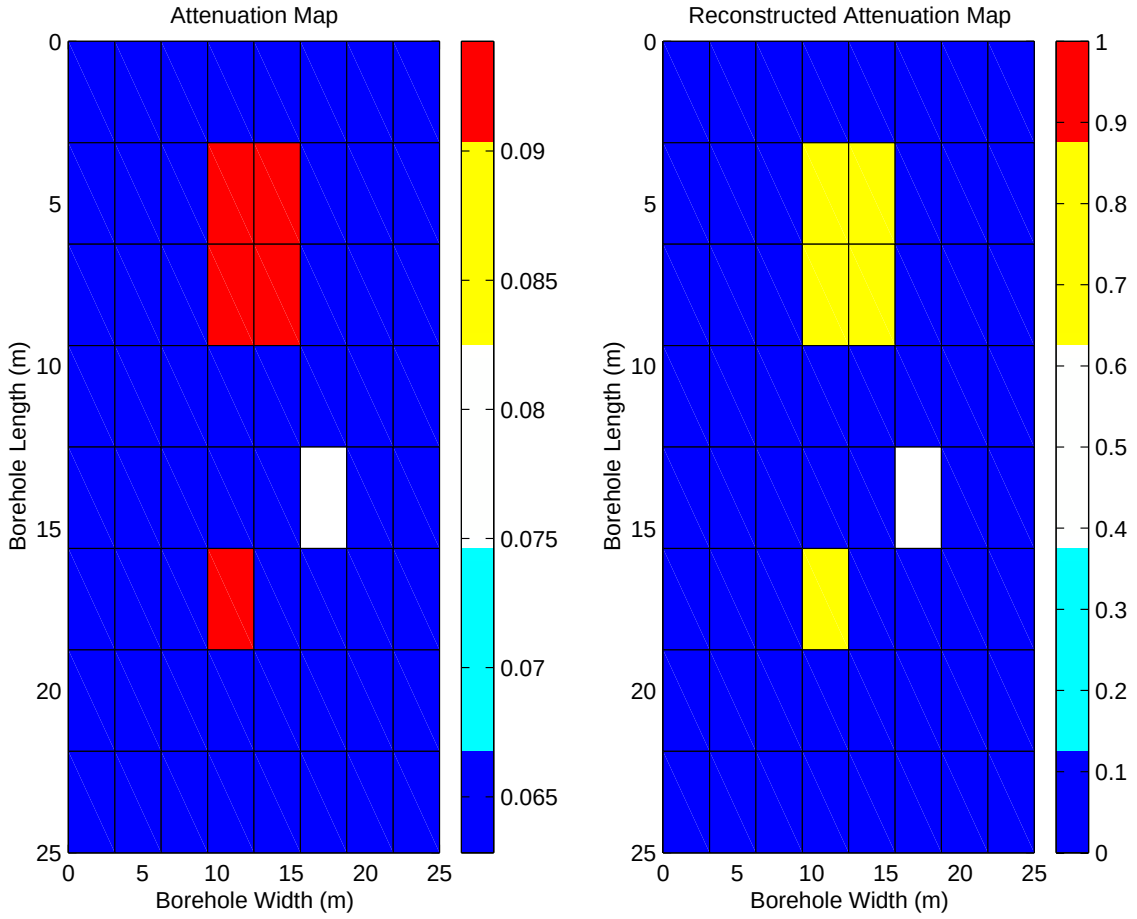

Figure 4.2: Simulated and Reconstructed Attenuation Map ($SNR = 67.78$dB)

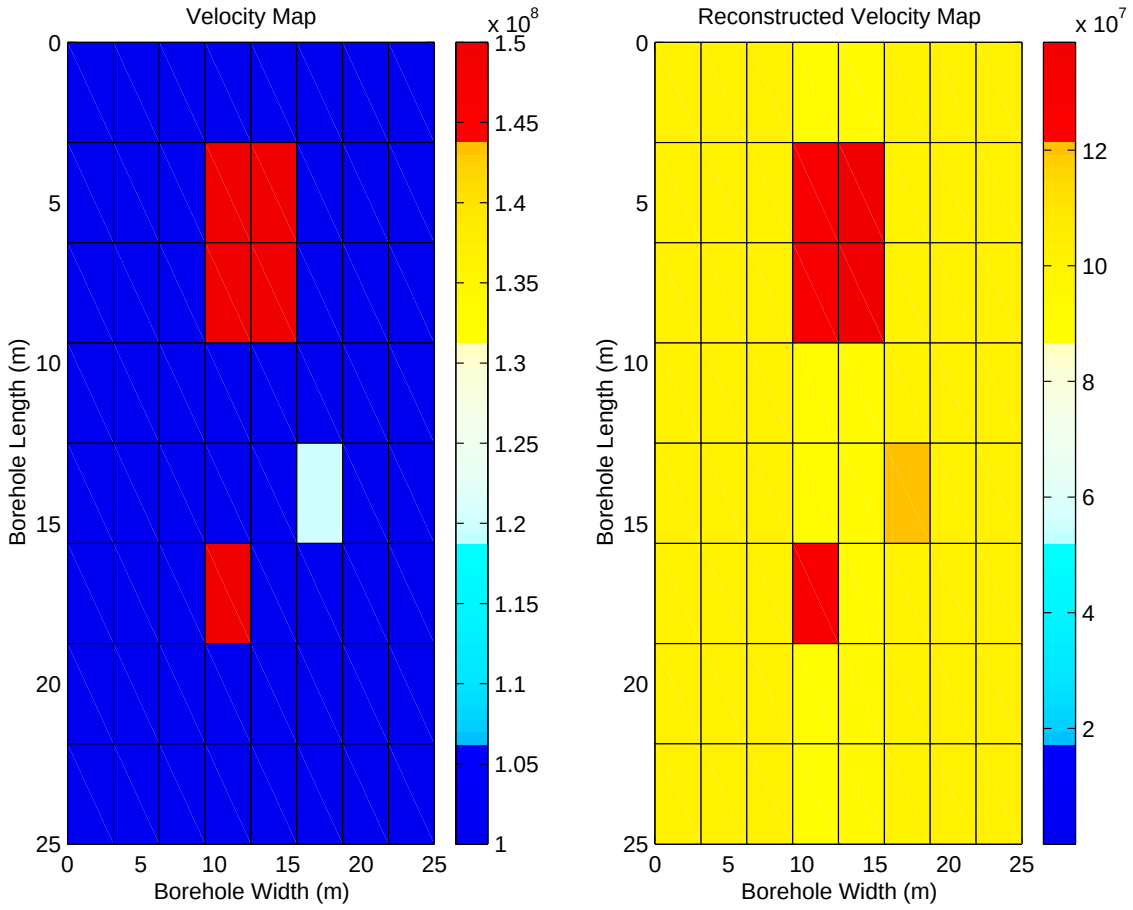

Figure 4.3: Simulated and Reconstructed Velocity Map ($SNR = 67.78$dB)

in the form of a plot. Finally, the thirteenth stage determines the unambiguous path length.

Stages seven to thirteen are discussed in more detail below.

4.3 ADC Resolution

The ADC resolution refers to the number of bits of the ADC. The resolution is determined from the following equation [21, page 122]:

$$SNR = 6.02B + 10.8 - 20log_{10}\left(\frac{X_m}{\sigma_x}\right) \tag{4.1}$$

In equation 4.1, SNR refers to the signal to noise ratio of the ADC, $B = N - 1$, where N represents the number of bits (ADC resolution), X_m represents the full-scale amplitude of the A/D converter, and σ_x is the rms value of the signal amplitude at the A/D converter. It is desirable to have X_m matched to ${\sigma_x}$[4].

The SNR is determined from the following equation [21, page 122]:

$$SNR = 10log_{10}\left(\frac{\sigma_x^2}{\sigma_e^2}\right) \tag{4.2}$$

Equation 4.1 is derived from this equation [21, page 122]. In equation 4.2, σ_x^2 represents the signal power, and σ_e^2 represents the noise power. This noise power is assumed to have a uniformly distributed probability density function [21, page 121], and therefore can be determined from the following equation [22, page 134]:

$$VAR[X] = \sigma_e^2 = \frac{(b-a)^2}{12} \tag{4.3}$$

In equation 4.3, b and a represent the upper, and lower bound values for the quantization noise, respectively.

The values from Table 4.1 were substituted into the above equations. The resultant SNR with these substituted values is 67.78dB, and the resultant ADC resolution is 10.97 bits, which rounds off to 12 bits, since 11 bit ADCs are not common. These particular values from Table 4.1 were utilised, because the values led to optimal

[4]Refer to section 4.5.

reconstruction of both the velocity, and the attenuation maps during the simulation process[5].

It is important to note that the ADC does not have to have a 12 bit resolution. It can utilise a lower resolution, and generate the same optimal reconstruction results, as above, by using the method of coherent integration [18, page 144]. This method takes a number of sampled values (phase, and amplitude) at each Rx position, and averages them. If an 8 bit ADC is utilised instead of a 12 bit ADC, then the SNR would drop to 49.9dB. The total number of sampled values, in each Rx position, required to bring the SNR back to 67.78dB, according to the simulation, is 61. This method is not implemented in this dissertation, because this hardware technology is relatively new, and therefore it is easier to establish a proven single sampled value coherent system first. A 12 bit ADC is utilised[6].

4.4 Tomographic Resolution

The radar resolution is dependent on the bandwidth of the transmit signal [23, page 15, and 17]. The radar range resolution refers to the minimum distance that the targets need to be from each other in order to detect two targets [23, page 15]. This explains the term radar resolution, but what is Tomographic resolution? Clearly, Cross-Borehole Tomography does not involve detecting targets, but rather producing subsurface images. Hence, the term Tomographic resolution must refer to the quality of the subsurface images reconstructed, but what effects the quality of these images?

In Figure 4.4, there are four Tx, and Rx positions. In Figure 4.5, there are six Tx, and Rx positions. In Figure 4.5, there are more ray paths, than in Figure 4.4. By looking at the Figures 4.4, and 4.5, it can be seen that if more Tx, and Rx positions are utilised then the area of ray coverage over the desired image region will be greater. Looking at equation 3.14, and 3.15 of Chapter 3, a subsurface image can only be reconstructed if the ray path passes through that part of the image region. In other words, the image region is pixelised, and these pixels each represent an unknown, which needs to be solved[7]. If there is no ray path through a pixel, then that particular unknown is cancelled out, and therefore the reconstructed image will not show that particular area of the image region. Hence, the quality of the

[5]Refer to section 4.7.
[6]Refer to section 4.7.
[7]Refer to Chapter 3.

reconstructed image will be poor. Therefore, the borehole geometry used in Figure 4.5 will result in a better quality reconstructed image than in Figure 4.4, because its geometry utilises more Tx, and Rx Positions, and therefore utilises a greater area of ray coverage.

The number of Tx, and Rx positions is not the only factor that effects the overall quality of the reconstructed subsurface image. In Figure 4.4, the image region is divided into an array of eight by eight pixels. This represents an array of 64 unknowns. In Figure 4.5, the image region is divided into an array of six by six pixels. This represents an array of 36 unknowns. In reality, the image region will be heterogenous in nature, and not homogenous as stated in this simulation. Therefore, the permittivity, and conductivity will vary throughout the image region, and hence the more unknowns (pixels) there are to solve for, the better the quality of the reconstructed image. This can be seen by looking at Figure 4.4, or 4.5. Take any pixel where the ray path passes through, and sub-divide it by a large number. Imagine that within that pixel the permittivity, and conductivity is varied. If a number of unknowns are utilised there is a greater chance of reconstructing this permittivity, and conductivity variance, yielding a better quality reconstructed image.

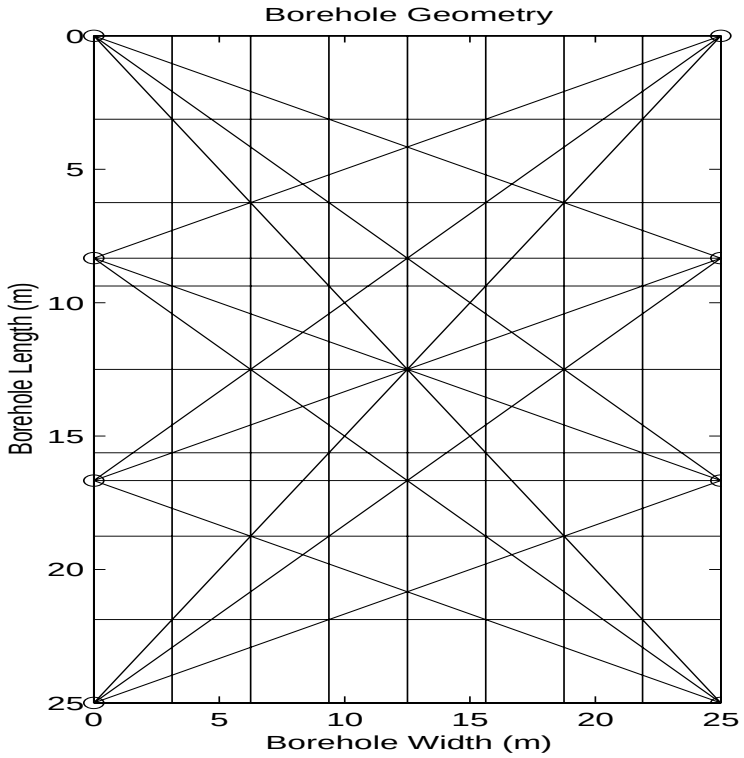

Figure 4.4: Borehole Geometry with Tx, and Rx Positions = 4

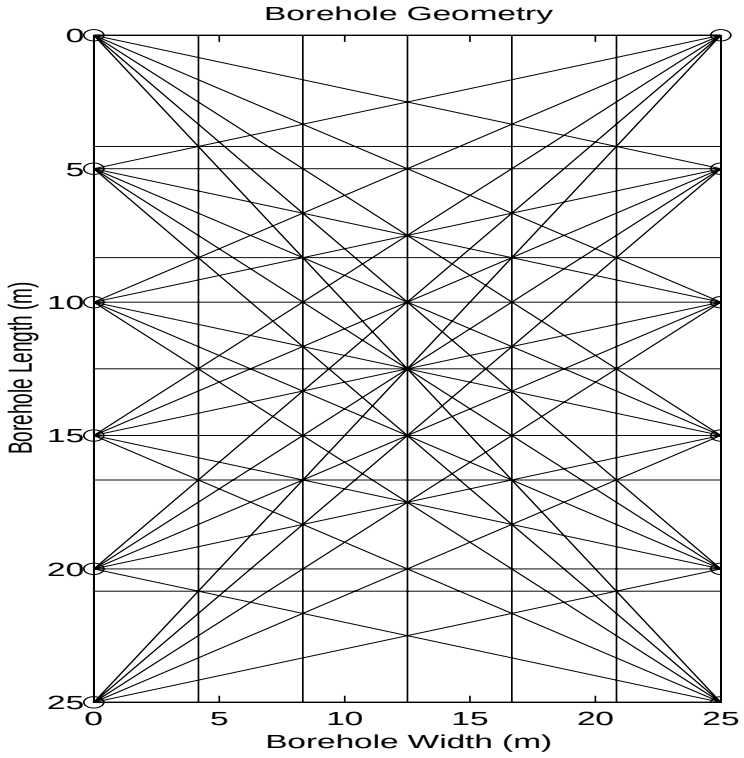

Figure 4.5: Borehole Geometry with Tx, and Rx Positions = 6

4.5 LNA Gain

The receiver hardware utilises a LNA[8]. Hence, the overall SNR at the receiver is improved. The LNA requires a gain such that the return signal is amplified to the full-scale range of the ADC [21, page 122]. This can be seen by looking at equation 4.1 in section 4.3. If the signal, σ_x, is too small then the term $-20log_{10}\left(\frac{X_m}{\sigma_x}\right)$ will become large, and negative, thereby reducing the overall SNR of the ADC [21, page 122]. If the signal, σ_x, is too large then it will exceed the full-scale value of the ADC causing clipping of the signal to occur, and hence the true signal's amplitude will be lost [21, page 122]. However, if $X_m \approx \sigma_x$ then the above term becomes $-20log_{10}(1)$, which is equal to zero [14]. This term is cancelled out, and therefore equation 4.1 now has an optimum SNR. Therefore, the LNA gain must be such that the input return signal is amplified, so that $X_m \approx \sigma_x$.

The results of the simulation for determining LNA gain can be found in Table 4.2, and Table 4.3[9]. In Table 4.2, the expected LNA gain for the first thirty-two ray path lengths is shown, and Table 4.3 shows the expected LNA gain for the last thirty-two

[8]Refer to Chapter 5.

[9]All input variables were taken from Table 4.1.

ray path lengths. There are sixty-four ray path lengths in total, because there are eight Tx, and eight Rx positions, as shown in Figure 4.1. These tabulated results show that the maximum LNA gain needs to be around 25.4dB, since Table 4.2, and Table 4.3 both show a maximum gain of 25.32dB.

Bear in mind that this simulation assumes that it is dealing with low-loss, non-magnetic media, and that the media consists of dry earth (sand)[10]. In a real environment the earth is likely to be moist, and the attenuation much greater[11]. Therefore, an LNA with a gain much greater than 25.32dB is needed in order to cater for the effects of the real environment.

4.6 Frequency Step Size

This section determines the frequency step size, and will show that the frequency step size is inversely proportional to the unambiguous path length.

The unambiguous path length refers to the ray path length where there are no phase ambiguities, much like unambiguous range in Radar systems [18, page 84]. The unambiguous path length in a non-stepped frequency system would be the length over which the overall phase change was less than, or equal to 2π [18, page 84]. This means that the wavelength of the transmit signal would have to be greater, or equal to the distance between the boreholes, and hence, limit the transmit frequency range capability[12].

The following equation is yielded for the unambiguous path length by looking at the equations for multiple frequency CW RADAR in Hovanessian's book [18, page 84-85], and assuming one way wave travel with the speed of light replaced with the velocity of the EM wave:

$$L_{unambig} = \frac{v}{\triangle f} \tag{4.4}$$

In equation 4.4, $L_{unambig}$ represents the unambiguous path length, $\triangle f$ represents the frequency step size, and v represents the velocity of the travelling EM wave[13]. It is clear to see from equation 4.4 that by making the frequency step size smaller

[10]Refer to section 4.2.
[11]Refer to Chapter 2.
[12]Refer to Chapter 3.
[13]Refer to Chapter 3.

Table 4.2: Return Values vs LNA Gain (1-32 Ray Path Lengths)

RETURN VALUES (V)	**LNA GAIN (dB)**
0.20787	19.6646
0.20458	19.8031
0.16749	21.5409
0.14622	22.7204
0.13063	23.6995
0.12313	24.2130
0.11342	24.9268
0.10845	25.3161
0.20458	19.8031
0.17081	21.3701
0.16778	21.5260
0.15915	21.9844
0.15701	22.1019
0.15218	22.3735
0.14232	22.9555
0.12632	23.9908
0.16749	21.5409
0.16778	21.5260
0.17081	21.3701
0.16778	21.5260
0.19521	20.2106
0.17347	21.2360
0.16379	21.7351
0.14163	22.9974
0.14622	22.7204
0.15915	21.9844
0.16778	21.5260
0.20787	19.6646
0.19663	20.1477
0.19126	20.3880
0.17471	21.1741
0.14627	22.7173

Table 4.3: Return Values vs LNA Gain (33-64 Ray Path Lengths)

RETURN VALUES (V)	**LNA GAIN (dB)**
0.13063	23.6995
0.15701	22.1019
0.19521	20.2106
0.20458	19.8031
0.19987	20.0057
0.18527	20.6646
0.17626	21.0975
0.17471	21.1741
0.12553	24.0453
0.15922	21.9806
0.18105	20.8648
0.18740	20.5653
0.17806	21.0091
0.18843	20.5174
0.20458	19.8031
0.19521	20.2106
0.11842	24.5524
0.14509	22.7878
0.15922	21.9806
0.15590	22.1637
0.17626	21.0975
0.20458	19.8031
0.20787	19.6646
0.20458	19.8031
0.10845	25.3161
0.11842	24.5524
0.12493	24.0873
0.14962	22.5208
0.18105	20.8648
0.19521	20.2106
0.20458	19.8031
0.20787	19.6646

increases the unambiguous path length.

A step frequency size of 2MHz[14], or smaller is utilised, because this yields an unambiguous path length of 50 metres, or greater, while displaying high quality image reconstruction[15]. The greatest path length that exists in the borehole geometry of Figure 4.1 is 35.355 metres (Pythagorean theorem: $\sqrt{25^2 + 25^2}$), and therefore 50 metres, or greater is more than ample in this case.

4.7 Phase vs Amplitude

4.7.1 Phase and Amplitude Extraction

The phase, and amplitude are extracted by using the IF sampling algorithm [16, page 33, and 34]. The IF signal is sampled at four times the IF frequency to extract the I, and Q samples. The IF frequency is set to 455kHz[16]. The received signal will not change over a specific ray path, because the permittivity, and the conductivity remain constant over the ray path, as is mentioned above. Thus, the waveform can also be sampled over more than one cycle. This is known as under sampling the waveform [16, page 33].

Figure 4.6 demonstrates the sampling process over a path length when sampling at four times the IF frequency, while utilising transmit frequency steps of 2MHz[17]. Figure 4.7 demonstrates the under sampling process over a path length, while utilising transmit frequency steps of 2MHz. The square wave represents the sampling signal, and the sinusoid represents the received signal at the ADC. The actual sample values are indicated by small circles where the square wave intersects the sinusoid on the positive edge of the square wave.

The I, and Q values are extracted from these samples by using the following equations [16, page 33, and 34]:

$$I = \frac{1}{4}\left(x\left[0\right] - x\left[2\right]\right) \tag{4.5}$$

$$Q = \frac{1}{4}\left(x\left[3\right] - x\left[1\right]\right) \tag{4.6}$$

[14] Refer to Table 4.1.
[15] Refer to Figure 4.2, and Figure 4.3.
[16] Refer to Chapter 5.
[17] Refer to Table 4.1.

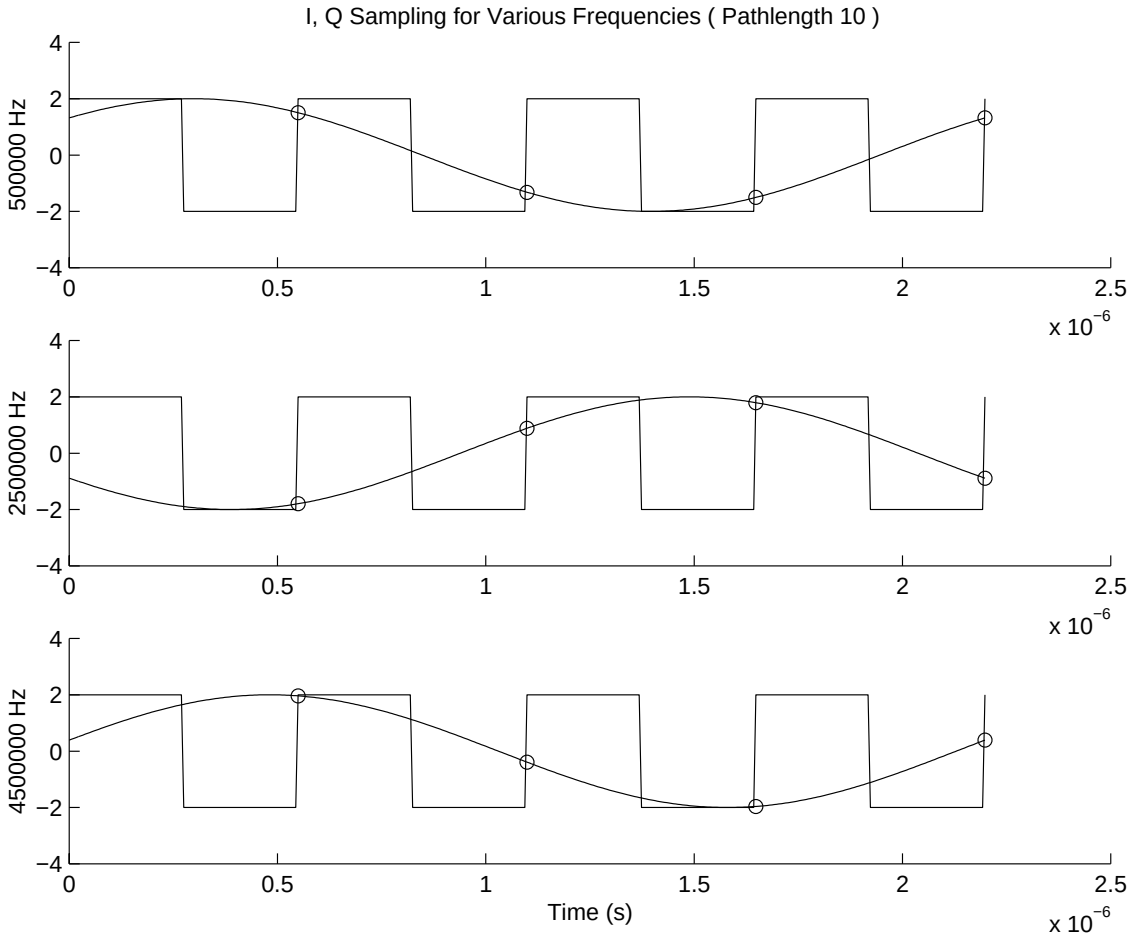

Figure 4.6: The Sampling Process (4xIF = 1.82MHz)

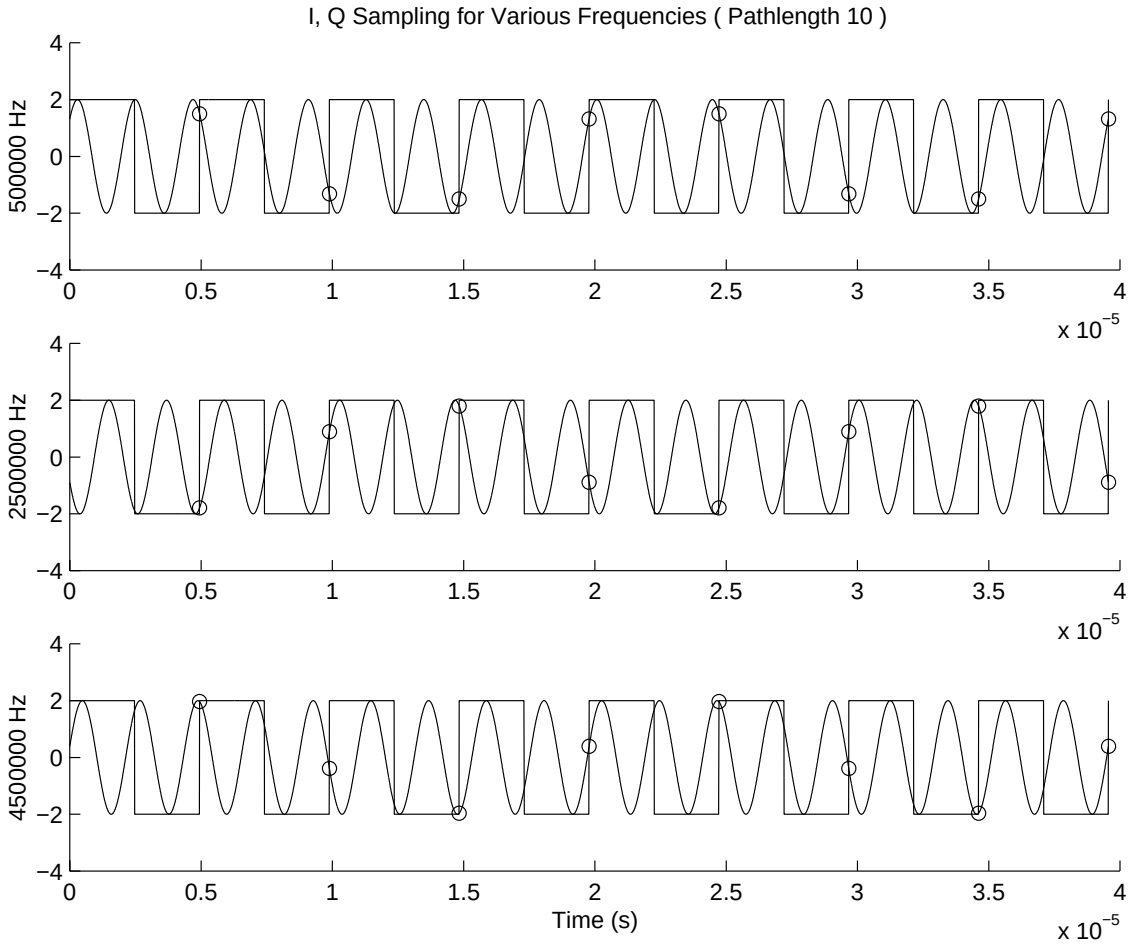

Figure 4.7: The Sampling Process (Under Sampling = 202.222kHz)

In equation 4.5, $x[0]$ represents sample 0, and $x[2]$ represents sample 2. In equation 4.6, $x[3]$ represents sample 3, and $x[1]$ represents sample 1. The phase, and amplitude is determined by using the following equations [16, page 33, and 34]:

$$\phi = \arctan\left(\frac{Q}{I}\right) \tag{4.7}$$

$$A = \sqrt{I^2 + Q^2} \tag{4.8}$$

In equation 4.7, the phase, ϕ, is determined by the quadrant it lies in. In equation 4.8, the amplitude, A, is half the expected amplitude, because multiplying two sinusoids together produces half the expected amplitude [16, page 34].

4.7.2 Attenuation and Velocity Reconstruction

The reconstruction process was implemented by using the Singular Value Decomposition (SVD) technique [20, page 61, and 62]. In Chapter 3, equation 3.14, and 3.15 essentially represent the following linear equation that needs to be solved [20, page 61]:

$$\mathbf{A} \bullet \mathbf{x} = \mathbf{b} \tag{4.9}$$

In equation 4.9, $\mathbf{A}$ represents a square matrix of pixel path lengths, $\mathbf{x}$ represents a vector of unknowns (velocity, or attenuation constants), and $\mathbf{b}$ represents a vector of receiver information (traveltime, or amplitude). In order to solve for $\mathbf{x}$, $\mathbf{A}$ needs to be invertible, or non-singular, and this would require $det\mathbf{A} \neq 0$ [19, page 28, and 29]. However, in this case, $\mathbf{A}$ is predominately filled with zeros, since the pixel path lengths of interest are the ones where the ray actually passes through the pixels. The rest are set to zero. This kind of matrix is an ill-conditioned, or not quite singular matrix, because the $det\mathbf{A} \approx 0$ [20, page 61]. This matrix appears to be invertible, but during the computational process of solving for $\mathbf{x}$ the $det\mathbf{A} = 0$, and the matrix $\mathbf{A}$ becomes invertible [20, page 61]. These sort of equations are solved by utilising numerical methods, such as the Iterative Methods technique[18]. The SVD technique works by identifying the values of $\mathbf{A}$ which make this matrix singular. It then eliminates the effect of these values by removing those equations which steers

[18]Refer to Chapter 2.

$\mathbf{x}$ away from its true value[19].

The attenuation, and velocity constants were both reconstructed with 12 bit ADC resolution, and 8 bit ADC Resolution. The 12 bit ADC's SNR is equal to 67.78dB, and the 8 bit ADC 's SNR is equal to 47.78dB. Figure 4.2 shows the attenuation reconstruction with the ADC's SNR equal to 67.78dB, and Figure 4.8 shows the attenuation reconstruction with the ADC's SNR equal to 47.78dB. Figure 4.2 shows fairly good image reconstruction quality, but Figure 4.8 shows some error in the reconstruction process, and yields a poorer quality image.

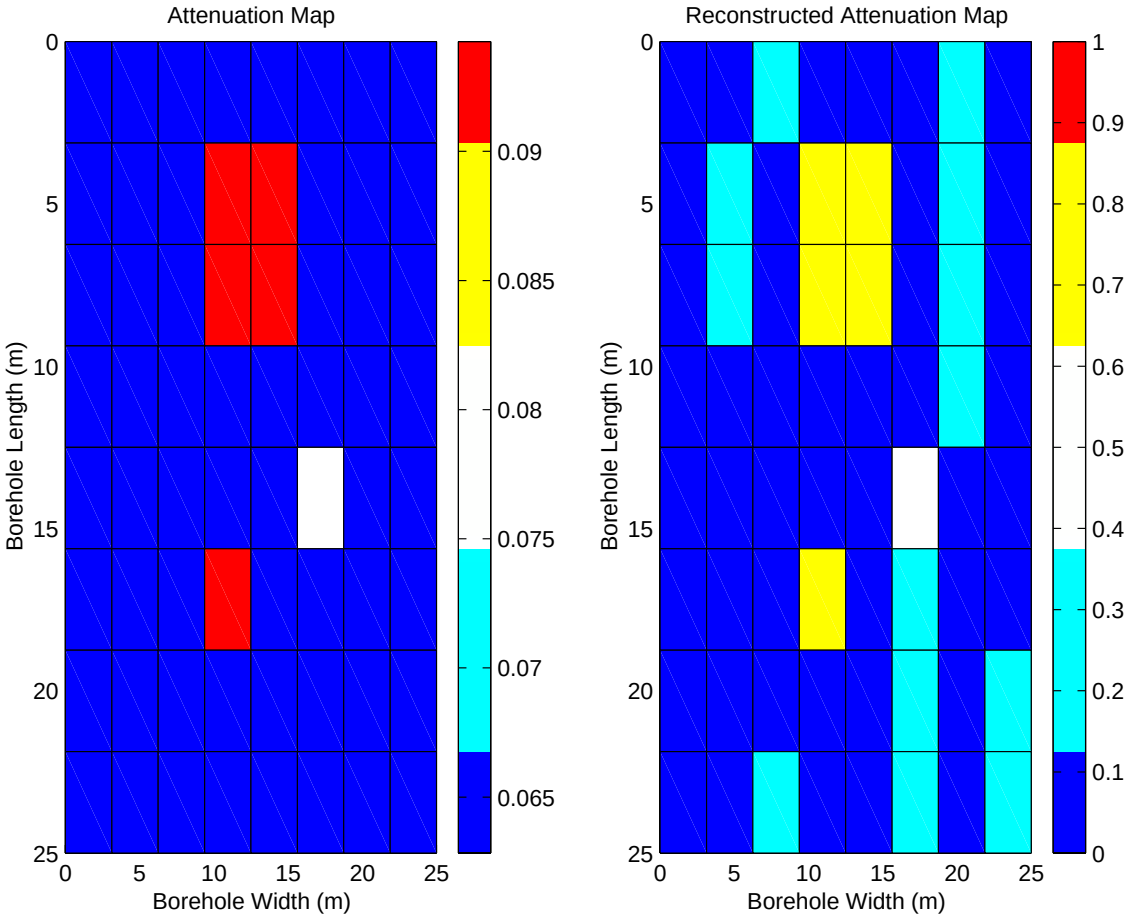

Figure 4.8: Simulated and Reconstructed Attenuation Map ($SNR = 47.78$dB)

Figure 4.3 shows the velocity reconstruction with the ADC's SNR equal to 67.78dB, and Figure 4.9 shows the velocity reconstruction with the ADC's SNR equal to 47.78dB. Figure 4.9 shows fairly good image reconstruction quality despite the decrease in the SNR. This can be more clearly understood by looking at the error plots in Figure 4.10, and Figure 4.11. In Figure 4.10, and 4.11, the top two plots illustrate the SVD least square error for attenuation, and velocity reconstruction with

[19]For more detail on the SVD algorithm refer to [20, page 61, and 62].

quantization noise equal to zero (ADC's SNR approaches ∞)[20]. This will produce a very high quality image. The SVD will always have an error, because SVD results in an approximation to the true value [20, page 62].

In Figure 4.10, the bottom two plots illustrate the SVD least square error for attenuation, and velocity reconstruction with the ADC's SNR equal to 67.78dB. The utilisation of an ADC with a 67.78dB SNR for both the attenuation, and the velocity maps has not distorted the SVD least square error values, and hence will result in a high quality image reconstruction, as seen in Figures 4.2, and 4.3.

In Figure 4.11, the bottom two plots illustrate the SVD least square error for attenuation, and velocity reconstruction with the ADC's SNR equal to 47.78dB. The utilisation of an ADC with a 47.78dB SNR has not effected the SVD least square velocity reconstruction error, but it has distorted the SVD least square attenuation reconstruction error, as seen in Figures 4.9, and 4.8, respectively. Hence, the attenuation reconstruction map will result in a poor quality image.

It seems the velocity reconstruction process can handle 12 bit, or 8 bit ADC resolution, but the attenuation reconstruction process can only handle 12 bit ADC resolution. Therefore, the phase information can handle an ADC with a lower SNR compared to the amplitude information, and hence, is able to produce an accurate velocity map image reconstruction even with an increase in noise.

A possible explanation for this could be that when stepping the transmit frequency, a larger phase shift is created, because phase is the accumulation of frequency over time[21]. Hence, utilising an ADC with a 47.78dB SNR would correspond to a small phase error, and adding a small phase error to a large phase shift would have a negligible effect. The phase error can be seen in Figures 4.12, and 4.13 for the ADC's SNR equal to 67.78dB, and 47.78dB, respectively. A 67.78dB SNR corresponds to a maximum phase error of 0.027 degrees, and a 47.78dB SNR corresponds to a maximum phase error of 0.3 degrees. However, if utilising the amplitude information (relatively small in magnitude), the increase in noise utilising the ADC with a 47.78dB SNR will effect the overall amplitude value, and hence, produce a poorer quality image.

The velocity reconstruction process can handle a phase error of 0.3 degrees, but when does the phase error begin to distort the velocity reconstruction process? This occurs when the ADC's SNR is equal to 42.68dB, as shown in Figures 4.14, and

[20] Refer to Equations 4.2, and 4.3.

[21] Refer to equation 3.23 in Chapter 3.

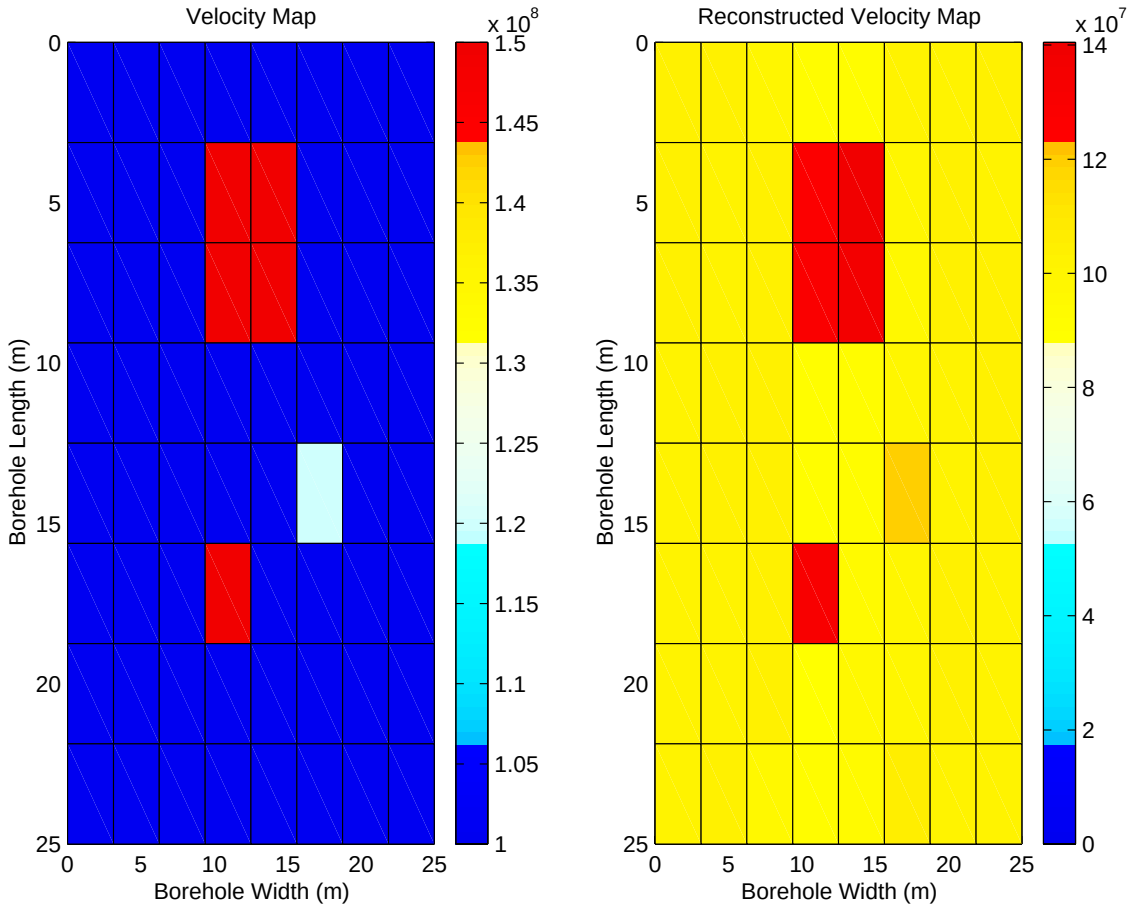

Figure 4.9: Simulated and Reconstructed Velocity Map ($SNR = 47.78$dB)

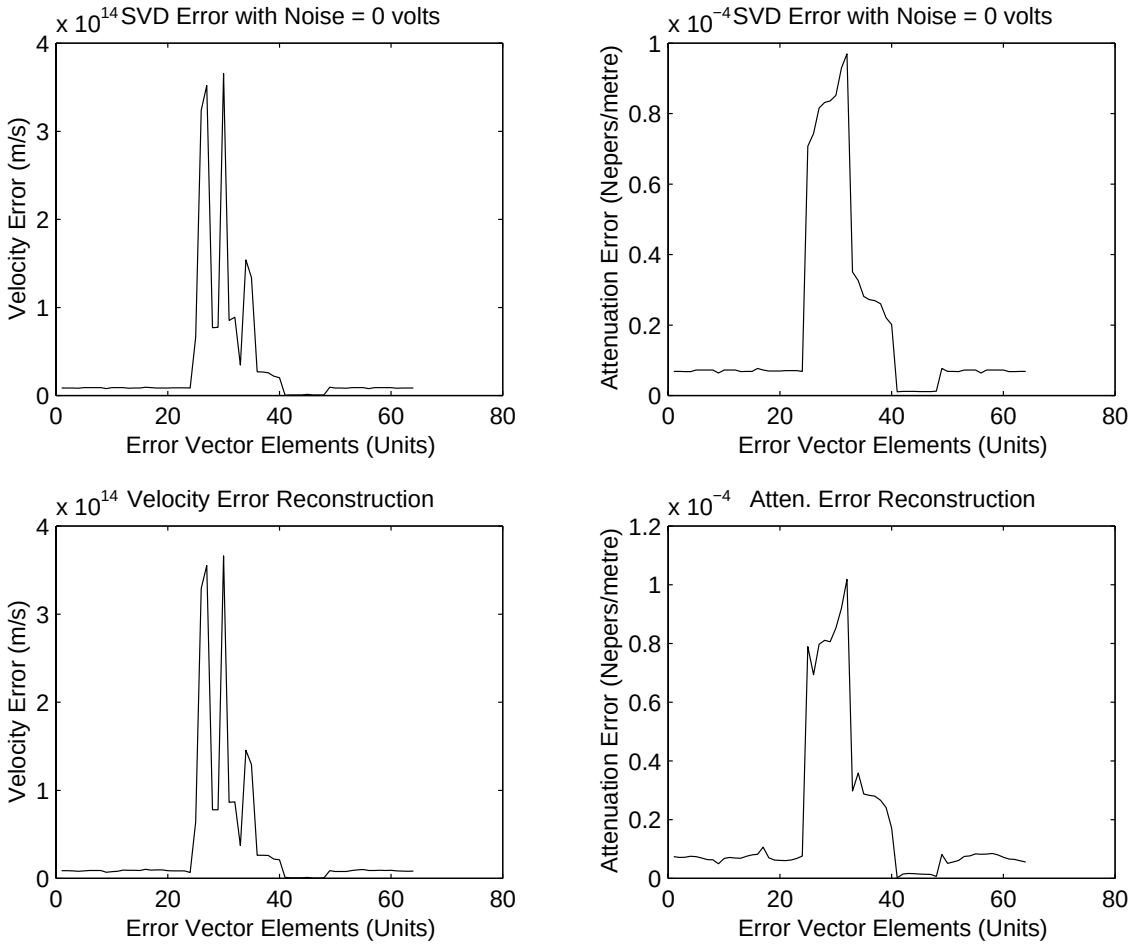

Figure 4.10: SVD Reconstruction Error ($SNR = 67.78$dB)

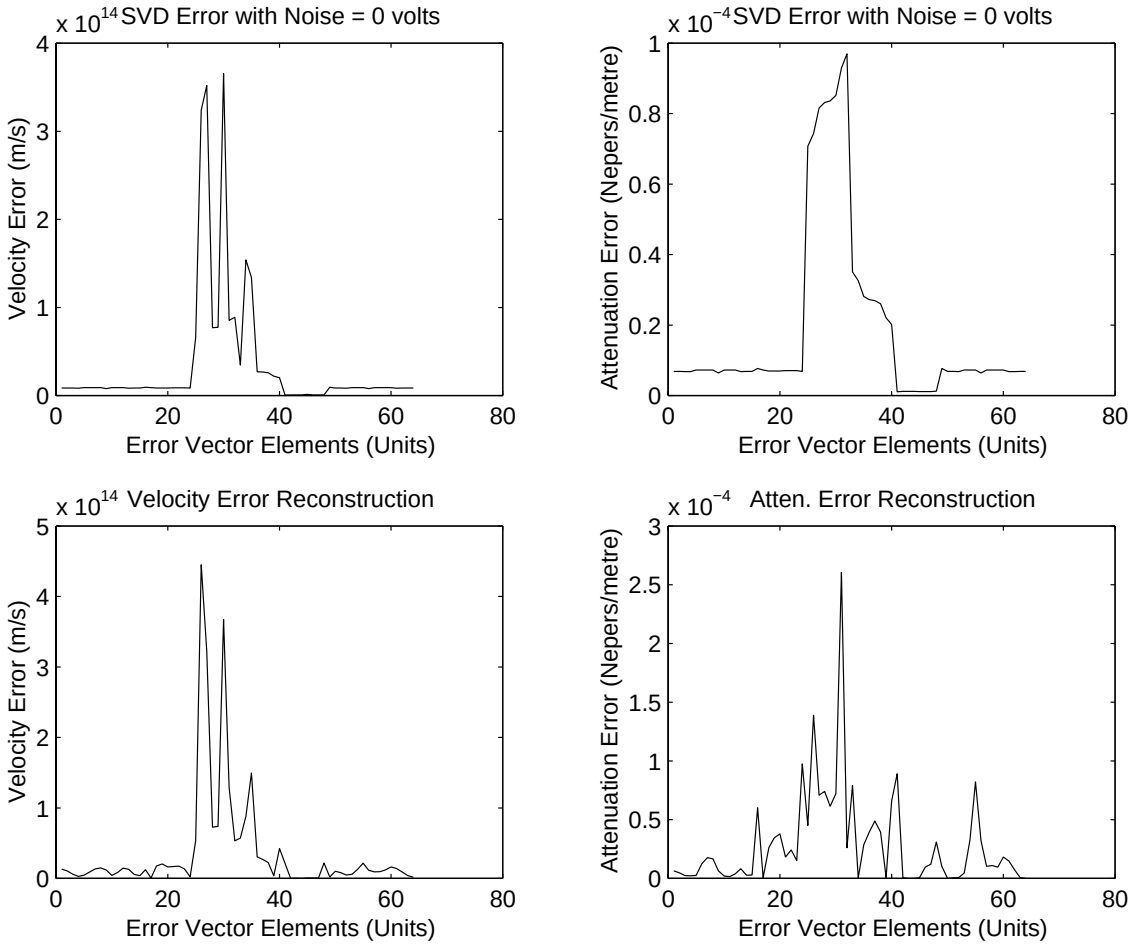

Figure 4.11: SVD Reconstruction Error ($SNR = 47.78$dB)

4.15. The maximum phase error in Figure 4.15 is 0.52 degrees. In general, it seems that when the phase error is greater than 0.4 degrees the velocity reconstructed image will become distorted.

Therefore, due to the above results, the hardware system will utilise an ADC with 12 bit resolution, and a minimum SNR equal to 67.78dB, because this results in high quality image reconstruction for both the attenuation, and the velocity maps.

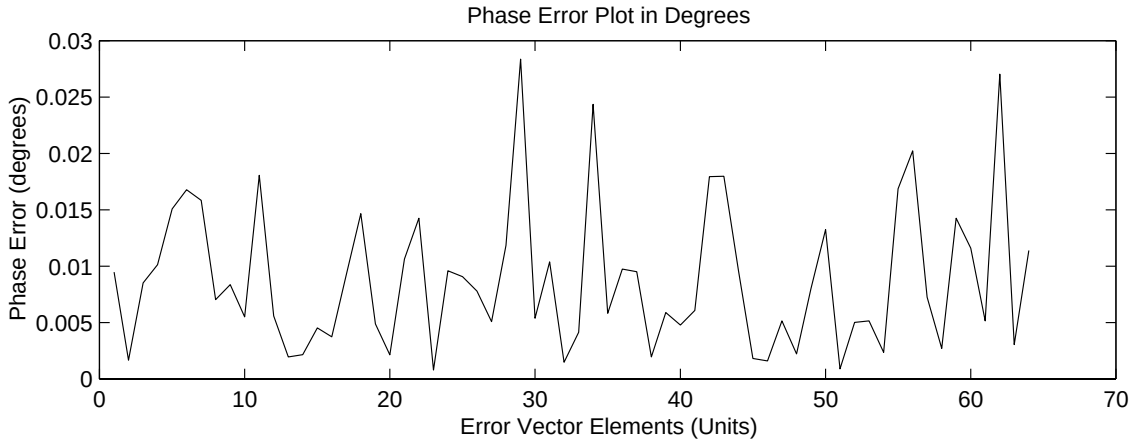

Figure 4.12: Phase Error ($SNR = 67.78$dB)

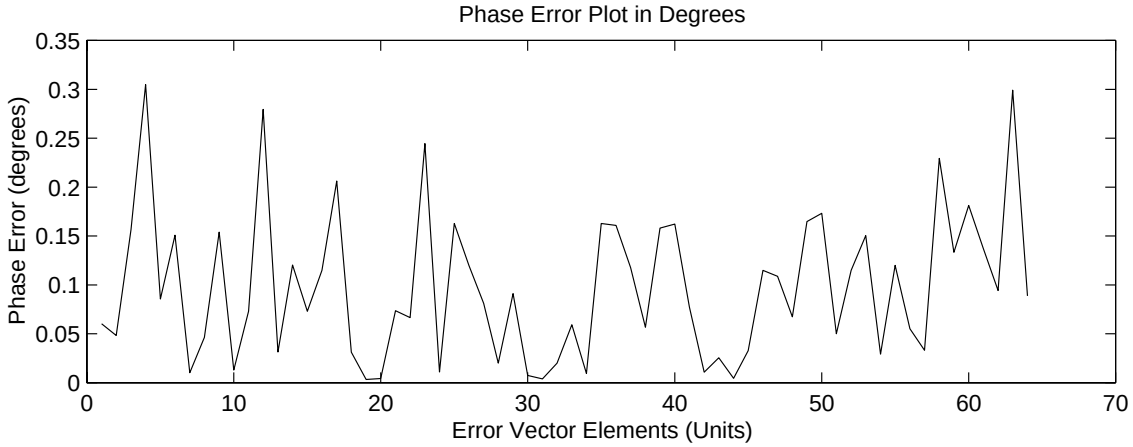

Figure 4.13: Phase Error ($SNR = 47.78$dB)

4.8 Conclusion

In conclusion, Tomographic resolution is dependent on the number of Tx, and Rx positions, as well as, the number of pixels. The greater the number of positions, and pixels utilised, the better the quality of the Tomographic image.

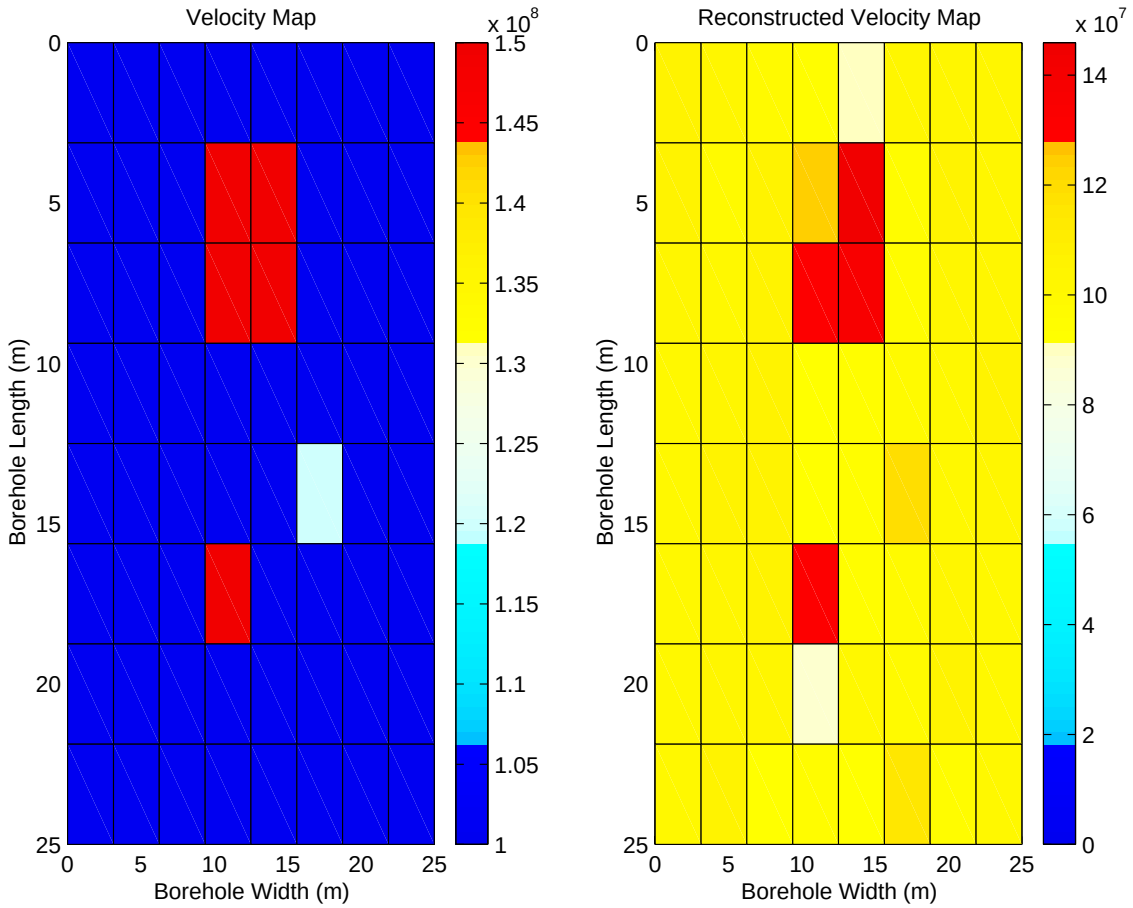

Figure 4.14: Simulated and Reconstructed Velocity Map ($SNR = 42.68$dB)

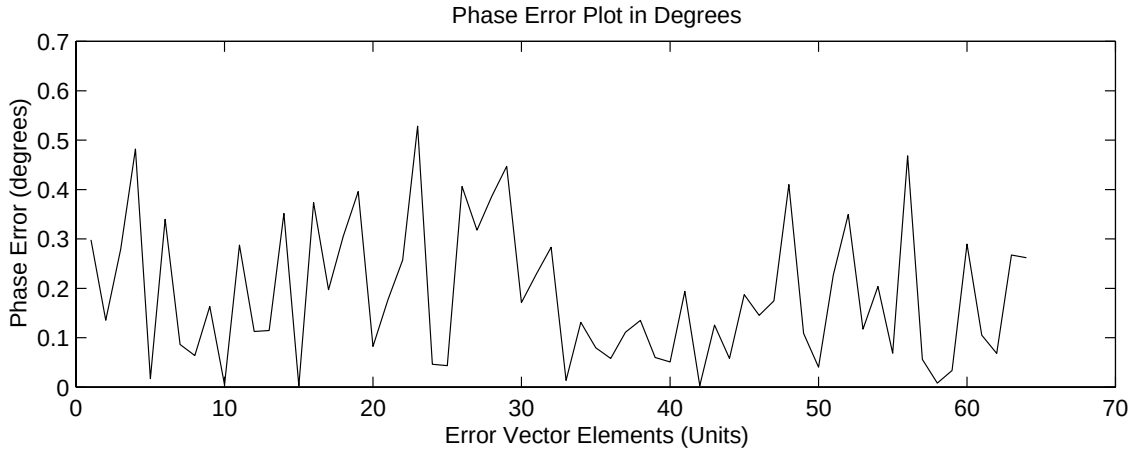

Figure 4.15: Phase Error ($SNR = 42.68$dB)

The frequency step size is inversely proportional to the unambiguous path length. Therefore, small frequency step sizes can increase the unambiguous path length, and hence, remove the transmit frequency range limitations encountered with non-stepped frequency systems, as discussed in chapter 3.

The phase information yields a better quality of image reconstruction when compared with the amplitude information. Hence, a coherent system is a good choice.

Chapter 5

Final Design

5.1 Introduction

This chapter begins by investigating three possible architectures for the final design: RF sampling, homodyne, and heterodyne. A decision is made as to which architecture this dissertation will utilise.

The system specifications are determined based on the user requirements for the dissertation, general mathematical analysis of receiver systems, the results of the Matlab simulation covered in Chapter 4, and other simulations.

The hardware, and software implementation of the final design is discussed in detail. The hardware consists of four main modules: Transmit Module, Receive Module, Control Module, and the PC Module. The software is explained by means of the flow diagrams in Appendix C.

Finally, this chapter explains how the system's coherent control is achieved.

5.2 Proposed Architectures

There are many different architectures which can be used to implement a CW, Stepped Frequency, Borehole, Tomographic Imaging system. This section explores the RF sampling, homodyne, and heterodyne architectures, discussing the advantages, and disadvantages of each architecture. A decision is made as to which of the above architectures will be utilised for this dissertation.

5.2.1 RF Sampling

The RF sampling architecture directly samples the RF receive signal, and performs the down-conversion to baseband, and the IQ signal generation in the digital domain [43, page 1]. This is achieved by having the ADC directly sample the receiver input RF signal, after some initial amplification, and bandpass filtering, as shown in Figure 5.1. The RF sampling eliminates the need for a mixer, synthesiser and other analogue circuitry in the receiver [43, page 1]. This is an advantage, because due to the use of fewer components the size of the receive PCB can be reduced to fit within a 47mm diameter borehole as specified in the user requirements statement[1]. The architecture is also cost effective, due to the overall reduction in components, and PCB size needed [43, page 1]. There is no DC offset, and I, Q channel imbalance that occurs with a homodyne system, as mentioned below[2].

The bandpass filter needs to have a wide bandwidth in order to accomodate the transmit frequency range of 500kHz to 5MHz, which is a user requirement[3]. This is a disadvantage, because outside interference can fall within this bandwidth, and mix with the receive signal, corrupting it [45, page 1]. The harmonics of the receive signal are not filtered out, and are also likely to mix with the receive signal. The ADC requires a high sampling rate in order to cater for wide bandwidth applications [44, page 57]. It is difficult to find an ADC with a high sampling rate, and a high resolution [44, page 57]. Therefore, an ADC with a high sampling rate may not have sufficient spurious free dynamic range [44, page 57].

5.2.2 Homodyne

A homodyne architecture mixes the receive signal with a copy of the transmit signal down to baseband (IF = 0Hz), as shown in Figure 5.2 [16, page 17]. This is a disadvantage, because the transmitter, and receiver modules are separated from each other, and would therefore require a link between each module[4]. This would make the system unnecessarily complicated, and non-modular, because the functionality of the receive module is dependent on the transmit module. It is also physically difficult to achieve a link between the transmit, and the receive module, as shown in Figure 2.1.

[1] Refer to section 1.1.
[2] Information supplied by Prof. M.R. Inggs.
[3] Refer to section 1.1.
[4] Refer to Figure 2.1.

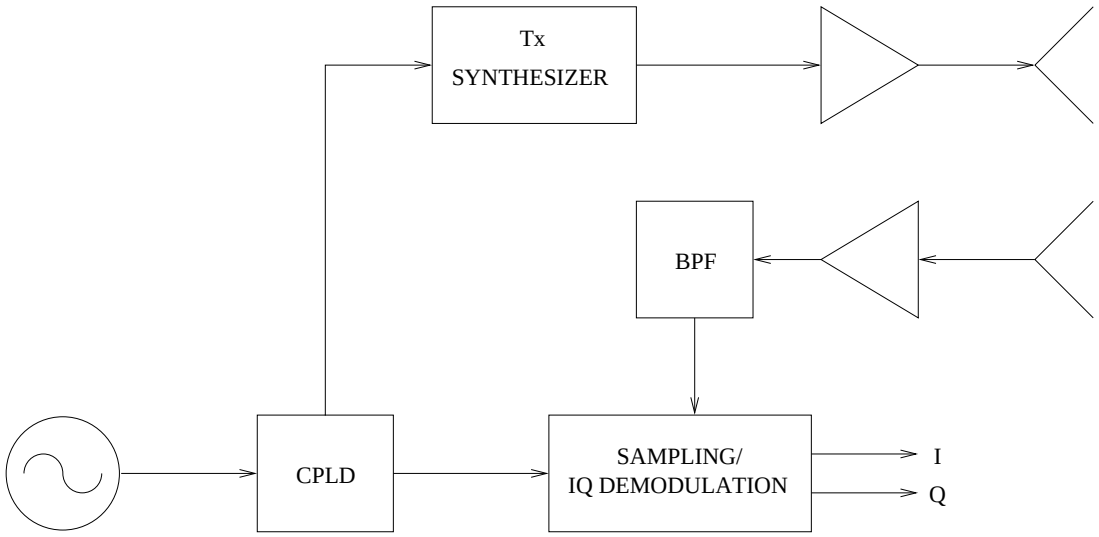

Figure 5.1: RF Sampling Architecture

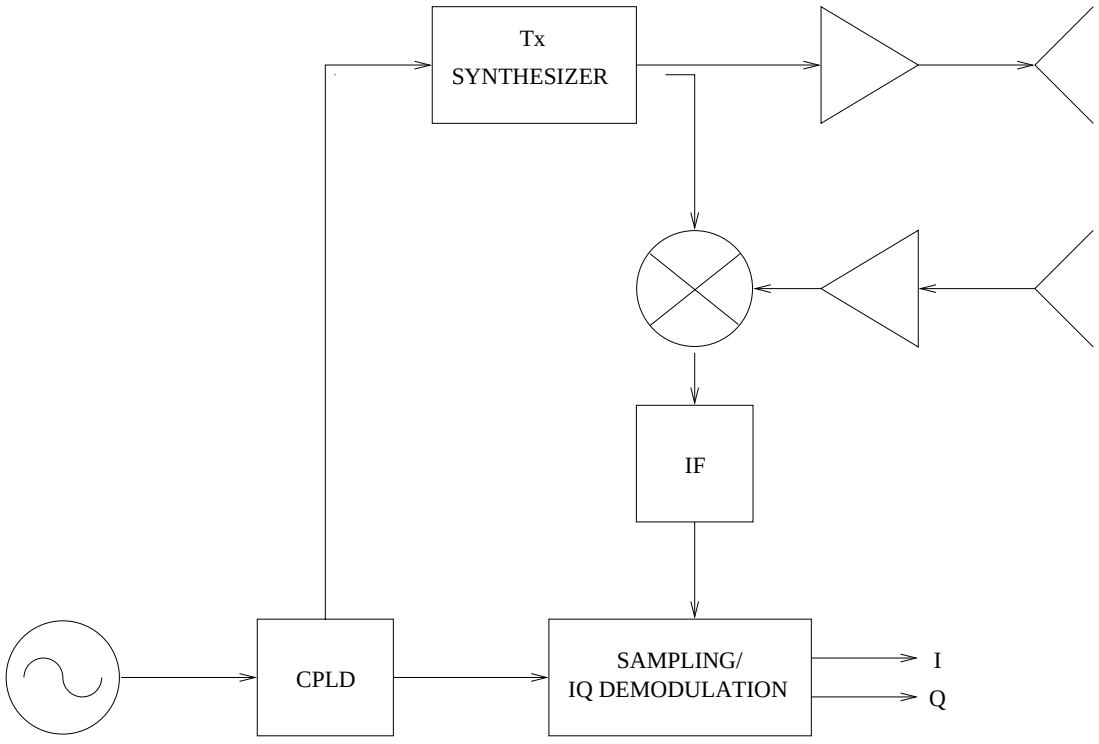

Figure 5.2: Homodyne Architecture

In theory, the mixer output contains information centered at baseband, and twice the transmitted signal frequency [16, page 17]. However, due to the mixer's non-linearities, harmonics at integer multiples of the transmitted signal frequency are also generated at the mixer output [16, page 18]. This is shown in Table 5.1, where f_t is the transmitted signal frequency. Both the upper, and lower sidebands are displayed up to the first two harmonics [16, page 18]. Table 5.1 shows that the harmonics are mixed down to baseband, and hence can corrupt the true signal information [16, page 18].

Table 5.1: Homodyne Mixer Output Harmonics

	f_t		$2f_t$		$3f_t$		...
f_t	0	$2f_t$	f_t	$3f_t$	$2f_t$	$4f_t$	...
$2f_t$	$-f_t$	$3f_t$	0	$4f_t$	f_t	$5f_t$	...
$3f_t$	$-2f_t$	$4f_t$	$-f_t$	$2f_t$	0	$6f_t$	...
$\vdots$	$\vdots$		$\vdots$		$\vdots$		$\ddots$

The other problem with homodyne architectures is that a quadrature demodulator module is required in order to extract the I, and Q values from the receive signal[16, page 19]. This requires the use of two ADCs for both I, and Q channels [16, page 19]. This introduces I, and Q errors through the quadrature demodulator, and the ADCs [16, page 19].

The baseband signal is also subject to flicker noise, and temperature drift [16, page 19]. The homodyne architecture is prone to many problems that are difficult to solve effectively, but it does normally have the advantage of utilising few components, and hence, the overall production cost is low [16, page 19].

5.2.3 Heterodyne

A heterodyne architecture mixes the receive signal with a signal that is offset in frequency from the transmit signal by the intermediate frequency, as shown in Figure 5.3 [16, page 19]. This is an advantage, because the problems of flicker noise, and temperature drift that occurs with homodyne architectures are eliminated, since the IF signal is no longer at baseband[5].

[5]Refer to section 5.2.2.

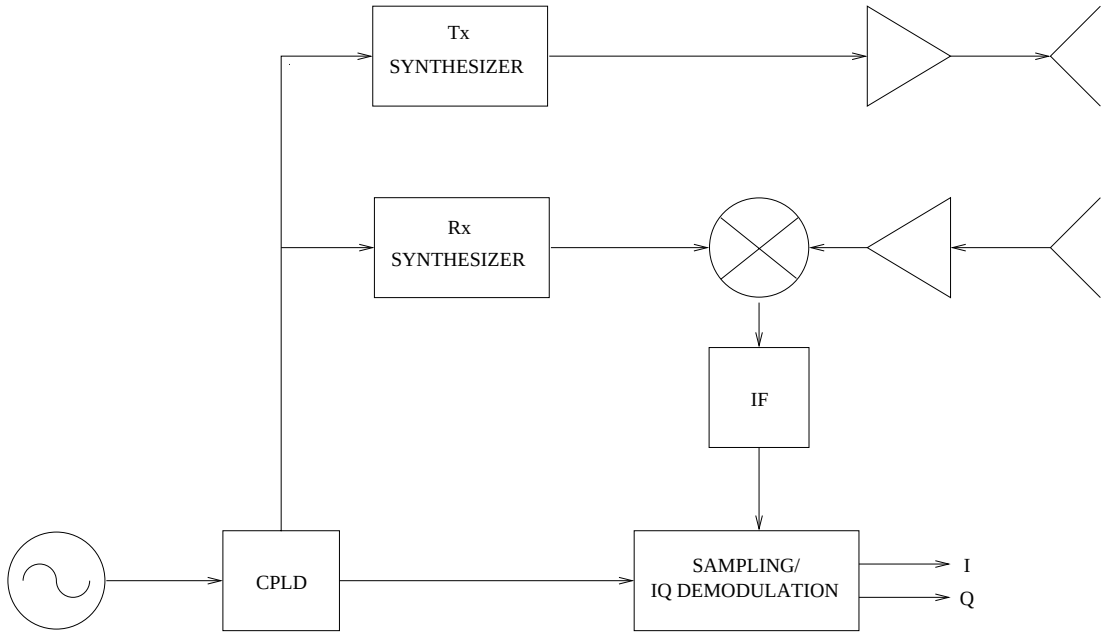

Figure 5.3: Heterodyne Architecture

The other advantage is that harmonics generated by the mixer output tend to mix down to outside the intermediate frequency, as shown in Table 5.2 where f_{if} represents the intermediate frequency, and f_t represents the transmitted signal frequency [16, page 20]. Only the lower sideband is considered. However, harmonics can still be mixed into the intermediate frequency bandwidth if the frequency step size of the synthesizers is not chosen correctly[6]. Therefore, the problem with the harmonics encountered in the RF sampling, and homodyne architectures is eliminated in the heterodyne architecture[7].

Table 5.2: Heterodyne Mixer Output Harmonics (Lower Sideband)

	Tx $= f_t$	Tx $= 2f_t$	Tx $= 3f_t$	...
Lo $= 1(f_t + f_{if})$	f_{if}	$-f_t + f_{if}$	$-2f_t + f_{if}$	...
Lo $= 2(f_t + f_{if})$	$f_t + 2f_{if}$	$2f_{if}$	$-f_t + 2f_{if}$	...
Lo $= 3(f_t + f_{if})$	$2f_t + 3f_{if}$	$f_t + 3f_{if}$	$3f_{if}$	...
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\ddots$

A further advantage is that the use of a quadrature demodulator module is no longer required, because the I, and Q values can be extracted using the IF sampling

[6]Refer to section 5.3.2.
[7]Refer to section 5.2.1, and 5.2.2.

technique discussed in the previous chapter[8] [16, page 20]. Hence, only a single ADC is needed, and therefore, the problem with the generation of the I, and Q errors found in the homodyne architecture is eliminated [16, page 20].

There are no real disadvantages to this system, except that it requires more components than the RF sampling architecture mentioned in section 5.2.1, and therefore may not be as cost effective, or compact.

This dissertation utilises the heterodyne architecture mainly because it does not experience the harmonic, or interference problems associated with the RF sampling, and homodyne architectures, mentioned in the above sections. The heterodyne system is also more compact than the homodyne system, because it requires only one ADC, and no quadrature demodulator module compared to the two ADCs, and one quadrature demodulator module of the homodyne system. It is desirable to have a compact system which can be utilised in 47mm diameter boreholes in order to meet the demands of the user requirements statement[9]. The heterodyne system has, in general, more advantages than disadvantages in comparison to the RF sampling, and homodyne architectures.

5.3 System Specifications

The following system specifications were determined by the user requirements for the dissertation, general mathematical analysis of receiver systems, the results of the Matlab simulation covered in Chapter 4, and other simulations.

5.3.1 IF Band and Transmit Bandwidth

The IF frequency is 455kHz, chosen because there are already available ceramic filter modules at this frequency, and hence the need to design a suitable BPF is no longer required [25].

The system is required to operate in a frequency range of 500kHz to 5MHz, which was specified in the user requirement statement[10].

[8] Refer to section 4.7.
[9] Refer to section 1.1.
[10] Refer to section 1.1.

5.3.2 Frequency Step Size and Receiver Bandwidth

A Matlab simulation was performed to determine which transmit frequencies generate mixer intermodulation harmonics (up to the 20th harmonic) closest to the IF band of interest[11]. The simulation was first performed with a frequency step size of 150kHz, and then with a frequency step size of 455kHz, as shown in Figures 5.4, and 5.5, respectively. In Figure 5.4, the closest harmonic actually lies in the IF band of interest. This occurs when transmitting at frequencies of 650kHz, and 4.55MHz. In Figure 5.5, the closest harmonic lies 45kHz away from the IF band of interest. This occurs when transmitting at frequencies of 555kHz, and 1.01MHz. Clearly, the choice of the frequency step size, and hence, the transmit frequency is important in terms of the intermodulation products generated at the mixer output.

Therefore, the frequency step size of choice is 455kHz, since this gives an unambiguous pathlength of greater than 50 metres, which far exceeds the required 35.355 metres, and also results in high quality image reconstruction[12]. The nearest harmonics are 45kHz, and 55kHz from the IF band of interest, but from then on the next closest harmonic is 100kHz away, as shown in Figure 5.5. This implies the transmit frequency range will result in IF-free harmonics, as shown in Figure 5.5.

The receiver bandwidth is determined by the IF filter (BPF) bandwidth [18, page 7]. The BPF bandwidth should be less than 90kHz in order to eliminate the effects of the harmonic $\pm$45kHz away from the IF band. The choice of bandwidth in this case is 21kHz [25].

5.3.3 LNA Gain

The LNA gain of choice is 40dB, because according to the results of the Matlab simulation in Chapter 4, a gain much greater than 25.4dB is needed in order to cater for the effects of the real environment[13]. The LNA of choice is the AD603 [26].

[11] File location on CD: D:\simulation\harmonic.m
[12] Refer to section 4.6.
[13] Refer to section 4.5.

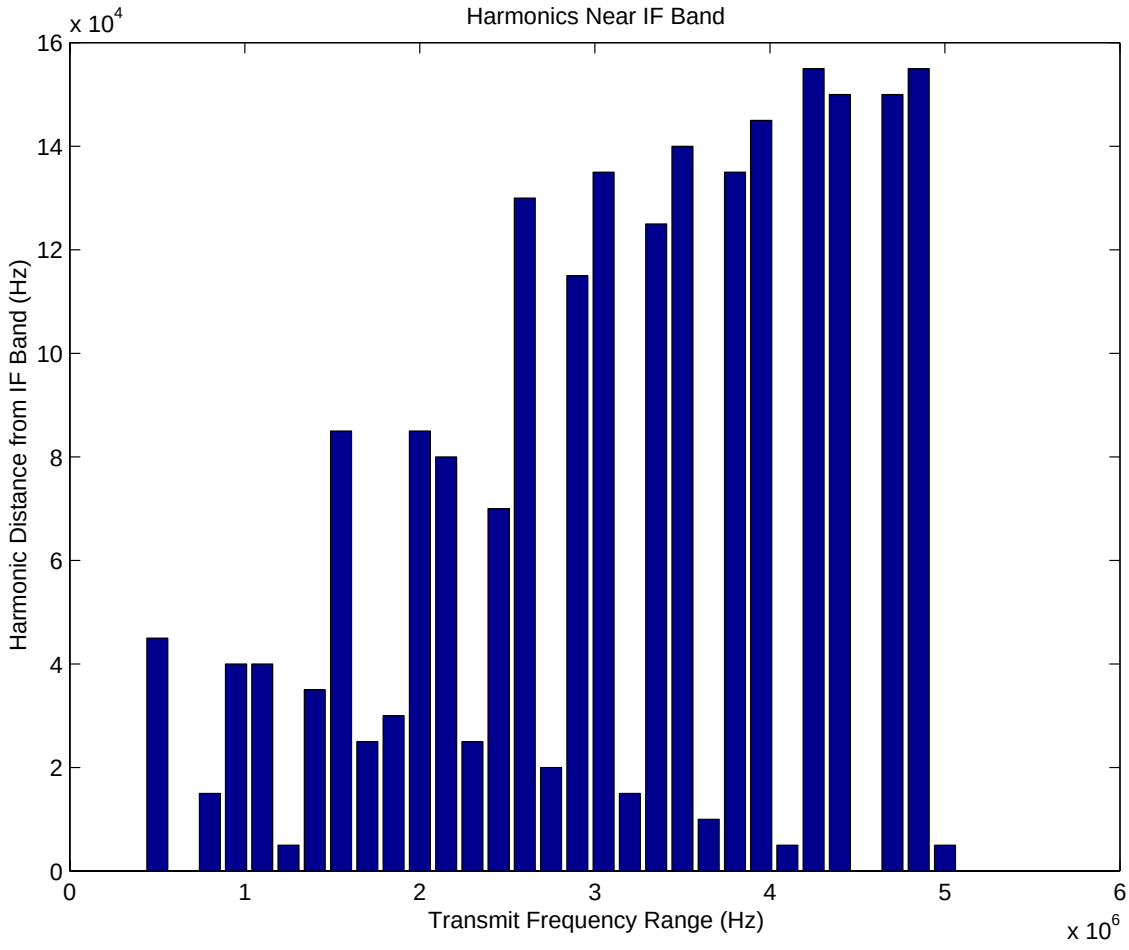

Figure 5.4: Harmonics Closest to the IF Band of Interest ($\triangle f = 150kHz$)

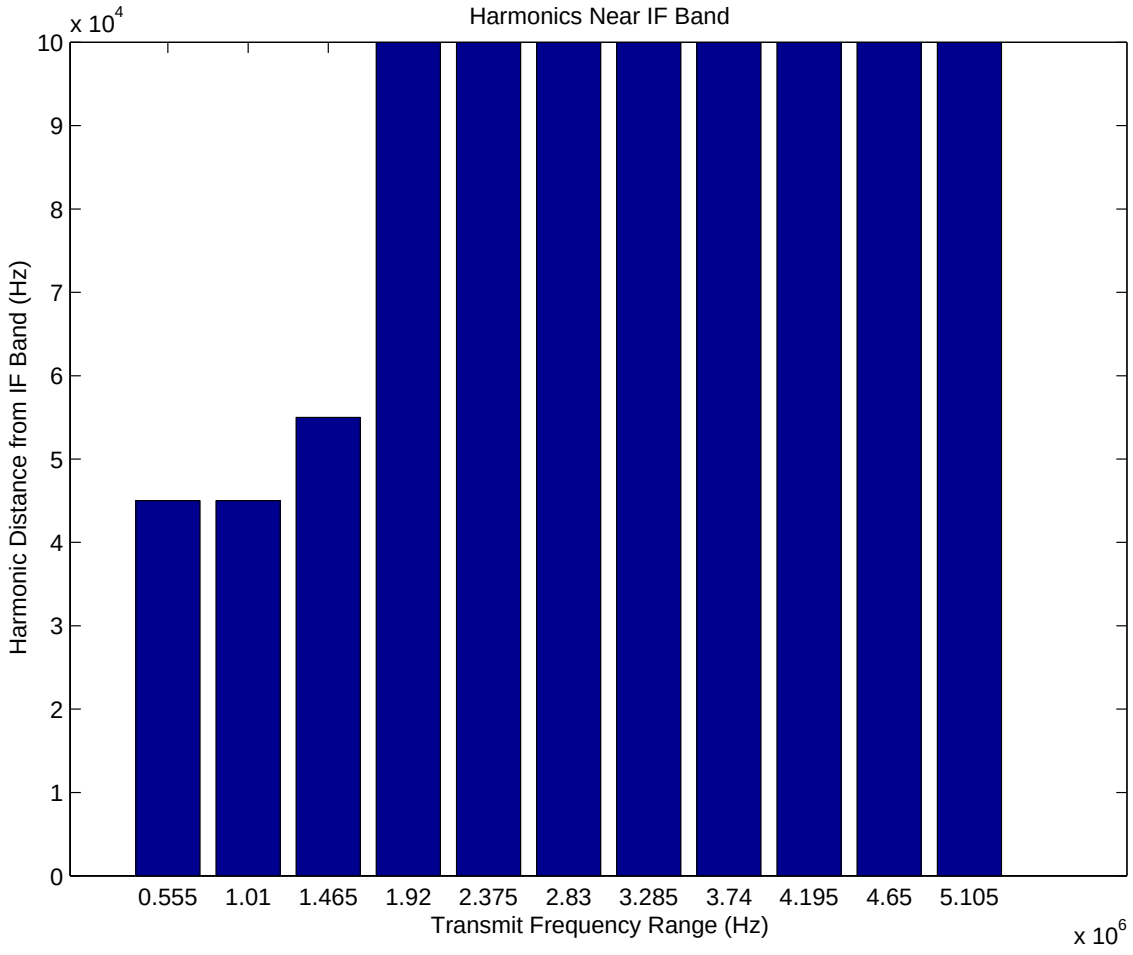

Figure 5.5: Harmonics Closest to the IF Band of Interest ($\triangle f = 455kHz$)

5.3.4 System Clocking

The master clock frequency must be a multiple of the sampling frequency, and the IF frequency[14] [16, page 29]. Therefore, it must either be a multiple of 1.82MHz (4 times the IF) or a multiple of 202.222 kHz (undersampling method)[15]. The undersampling method is utilised in this case in order to lower the ADC sampling requirements needed, and hence, result in a cost effective ADC [27]. The master clock frequency is chosen to be 58.24MHz, which is 288 times, and 128 times the sampling frequency, and the IF frequency, respectively.

The ADC chosen requires a clock frequency that is sixteen times the sampling frequency [27, page 17]. Hence, the master clock frequency divided by 18 is used as the ADC clock, as shown by ADC CLOCK in Figure 5.9.

The master clock frequency going to the synthesizer needs to be large enough in order to reduce the phase noise at the output [24, page 9]. The AD9851 synthesiser has a six times reference clock multiplier on board, so it can accept lower clock frequencies [24, page 9]. The fundamental output frequency should be limited to 40% of the reference clock frequency in order to prevent aliased signals getting too close to the band of interest [24, page 9]. The synthesiser clock is multiplied up to 58.24MHz (9.707MHz x 6), and 40% of this frequency is 23.296MHz. Therefore, the transmit range of 500kHz to 5MHz, and the local oscillator range of 955kHz to 5.455MHz is safe from aliased signals.

The clock to the microcontroller needs to be chosen such that the baud rate error is low enough (5% error is allowed) [16, page 29]. A Matlab simulation was performed in order to work out the baud rate errors for respective baud rates, and their clock frequencies[16]. A crystal clock frequency of 4.608MHz is used for the microcontrollers, because this yielded a baud rate error of zero for 2400bps, 9600bps, 14400bps, 28800bps, 19200bps, and 57600bps. A baud rate of 38400bps yields a 6.67% error, and a baud rate of 115200bps yields a 20% error for this particular clock frequency. The system utilises a baud rate of 2400bps. The clock frequency of 4.608MHz was chosen, because crystals in this frequency are easily available off the shelf.

[14] Refer to section 5.5.
[15] Refer to section 4.7.
[16] File location on CD: D:\simulation\AVRbaud.m

5.3.5 Transmit Power

The transmit power is 10dBm, because this falls within the power range specified in the user requirement statement[17].

5.3.6 ADC Dynamic Range, Resolution and Full-Scale Value

The ADC dynamic range, which is effectively the signal-to-noise ratio, is defined as the maximum signal power the ADC can handle before clipping occurs less the quantization noise power [21, page 122]. The simulation in Chapter 4 showed that the ADC needed to have a dynamic range of 67.78dB, a 12 bit resolution, and a full-scale amplitude value of 2 volts in order to produce a high quality image for both the attenuation and velocity reconstruction processes[18]. The ADC chosen to meet these requirements is the LTC1404 [27, page 1]. It has a dynamic range of 72dB, a 12 bit resolution, and a full-scale amplitude value of 2.048V.

5.3.7 Receiver Dynamic Range

The compression-free dynamic range is defined as the 1dB compression point of the system less the power associated with the minimum detectable signal within the receiver bandwidth [29, page 17.6]. The dynamic range is calculated using the following formula [29, page 17.6]:

$$DR = P_{1dB} - P_{min} \tag{5.1}$$

In equation 5.1, DR represents the compression-free dynamic range, P_{1dB} represents the 1dB compression point, and P_{min} represents the minimum detectable signal within the receiver bandwidth. P_{1dB} is determined by the LNA, and represents the point where the output falls 1dB from its linear region as the amplifer starts to saturate [29, page 17.6]. The AD603 has a 1dB compression point of -11dBm (referred to the input) [26, page 2]. P_{min} is determined by the noise power [29, page 17.6, and 17.7]. The noise power is given by the following equation [29, page 17.6]:

[17] Refer to section 1.1.
[18] Refer to section 4.3 and 4.7.2.

$$P_{min} = k + T + B + F \tag{5.2}$$

In equation 5.2, k is the boltzmann's constant, T is the absolute temperature, B is the bandwidth of the receiver[19], and F is the overall noise figure of the receiver. Equation 5.2 can also be expressed in terms of the equivalent noise temperature instead of the noise figure, but this is only really necessary at the microwave frequencies where really low noise levels, and low noise figures are encountered [29, page 17.42]. The overall noise figure of the receiver is given by the following equation [30, page 201]:

$$F_t = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + ... \tag{5.3}$$

In equation 5.3, F_1 to F_3 represent the noise figures for gain stages G_1 to G_3, respectively. The first stage (F_1, G_1) represents the LNA. The LNA has a noise figure of 8.8dB (referred to the input), and a gain of 40dB [26, page 2]. In this case, F_t is dependent on F_1, because $G_1 \gg 1$ [30, page 201]. Therefore, the last two remaining terms in equation 5.3 are reduced to zero. Hence, P_{min} can now be determined by substituting k, T, B, and F into equation 5.2 to yield the following:

$$P_{min} = 10log(1.38 \times 10^{-23}) + 10log(290) + 10log(21000) + 8.8 = -121.96dBm$$

Therefore, DR can now be determined by substituting P_{1dB}, and P_{min} into equation 5.1 to yield the following:

$$DR = -11dBm + 121.96dBm = 110.96dB$$

The compression-free dynamic range is fairly large, but this is the ideal dynamic range, and in the real world the dynamic range is likely to be lower than 100dB[20]. The compression-free dynamic range assumes that the receiver only has a single signal at the input, and that it is a desired signal [46, page 1]. It does not take into account interfering signals that are likely to lower the overall dynamic range [46, page 1].

[19] Refer to section 5.3.2.

[20] Information supplied by RF Design Engineer, Paul Fourie, from Reutech Radar Systems.

5.3.8 Receiver Sensitivity

The signal power level that is equal to the noise floor power, P_{min}, as mentioned in section 5.3.7, is referred to as the minimum detectable signal (MDS) [29, page 17.5]. The receiver sensitivity value is considered to be 9.54dB above the noise floor power [29, page 17.5]. The receiver sensitivity is therefore defined as the input value (dBm) that increases the total output (signal + noise) value by 10dB [29, page 17.5]. Hence, the receiver sensitivity can be determined by the following equation [29, page 17.5]:

$$S(dBm) = P_{min} + 9.54dB \tag{5.4}$$

The receiver sensitivity, $S(dBm)$, can now be determined by substituting P_{min} into equation 5.4 to yield the following:

$$S(dBm) = -121.96dBm + 9.54dB = -112.42dBm$$

The receiver sensitivity value is fairly low, and adequate in this case considering that the signal through the simulated environment in Chapter 4 did not experience a severe amount of attenuation[21]. Therefore, the minimum received signal is always likely to be greater than -112.42dBm when operating in the same environment as the simulated environment covered in Chapter 4.

5.3.9 Power Consumption

The Maximum Power Consumption for the various modules[22] can be seen in Table 5.3. Table 5.3 was determined by looking at the power consumption for each active component on each module [24], [26], [27], [28], [29], [32], [33], [34], [35], [37], [39], [40], [41], [42].

Each module is designed to be powered up by rechargeable batteries connected to the module's DC to DC converter (LT1376-5), which generates the required voltage [34]. The choice of battery type, and size for the Transmit, and Receive Modules is very important, because the batteries need to operate in extreme temperatures,

[21] Refer to section 4.5.
[22] Refer to section 5.4.

and in 47mm diameter boreholes[23] . The Control Module is not limited by size[24].

However, for this dissertation, a power supply will be used to provide power to each Module instead of the DC to DC converters, and rechargeable batteries. The power supply must be able to supply a voltage range of ±5 volts, and a maximum current of 2A[25].

Table 5.3: Maximum Power Consumption

	Power	Current	Volts
Control Module	2.86W	571.0mA	+5V
Transmit Module	1.74W	345.7mA	±5V
Receive Module	2.29W	402.3mA	±5V

5.3.10 Temperature Range

The system is designed to operate in the temperature range of 0^oC to 70^oC, even though some components can handle a wider temperature range [24], [26], [27], [28], [29], [32], [33], [34], [35], [37], [39], [40], [41], [42]. Higher temperatures would require heat dissipation techniques[26] .

5.3.11 Board Dimensions

The PCB dimensions for the various modules can be seen in Table 5.4. The Transmit Module PCB, and Receive Module PCB both require a width much less than the 47mm borehole diameter specified in the user requirements statement in order to make provision for the mechanical structure that encloses the PCBs[27].

However, in this dissertation, no mechanical structure is designed, or implemented, because the idea is to demonstrate that a coherent system can be achieved, rather than be utilised in the field[28].

[23]Refer to section 1.1 and 2.3.
[24]Refer to section 5.4.
[25]Refer to Table 5.3.
[26]Refer to section 2.3.
[27]Refer to section 1.1.
[28]Refer to section 1.1.

Table 5.4: Board Dimensions

	Length (mm)	Width (mm)
Control Module PCB	152	70
Transmit Module PCB	203	25
Receive Module PCB	230	29

5.4 Hardware and Software Implementation

This section discusses the functionality, as well as, the implementation of the hardware, and software design for this dissertation. The hardware consists of four modules: Control Module, Transmit Module, Receive Module, and PC Module, as shown in Figure 5.6. A digital photograph of the final PCB hardware system is shown in Figure 5.7. In Figure 5.7, the Control Module is located at the top, the Transmit Module is located to the left, and the Receive Module is located to the right.

The Control Module, Transmit Module, and Receive Module are controlled by on-board microcontrollers, which run C embedded code [28, page 3-3 and 6-3]. The PC Module can be a lap-top, or any standard PC that can run a Java 1.2 Swing application[29]. The C embedded code, and Java Swing application code is explained in terms of the flow diagrams found in Appendix C.

5.4.1 Control Module

The Control Module consists of the following main components: microcontroller, position control interface, and a CPLD, as shown in Figure 5.8. The schematic can be found in Figure A.1. The PCB can be found on the CD[30]. This module will remain on the surface, and will interface with the PC Module via a RS232 serial link, as well as, the Transmit, and Receive Modules via fiber-optics, as shown in Figure 5.6, and 5.8, respectively.

The Control Module generates the master clock[31], which is divided down by six in the CPLD, and fed through to both the Transmit Module, and the Receive Module via the 10 Megabaud fiber-optics modules [39], [40]. The CPLD (EPM7128STC100-15) provides good clock, and transmit signal buffering[32] [38]. The transmit signal is

[29]Refer to any Java site, e.g., http://java.sun.com/
[30]File location on CD: D:\Hardware\Control\PCB\Control.pdf
[31]Refer to section 5.3.4.
[32]Information supplied by Dr. Alan Langman.

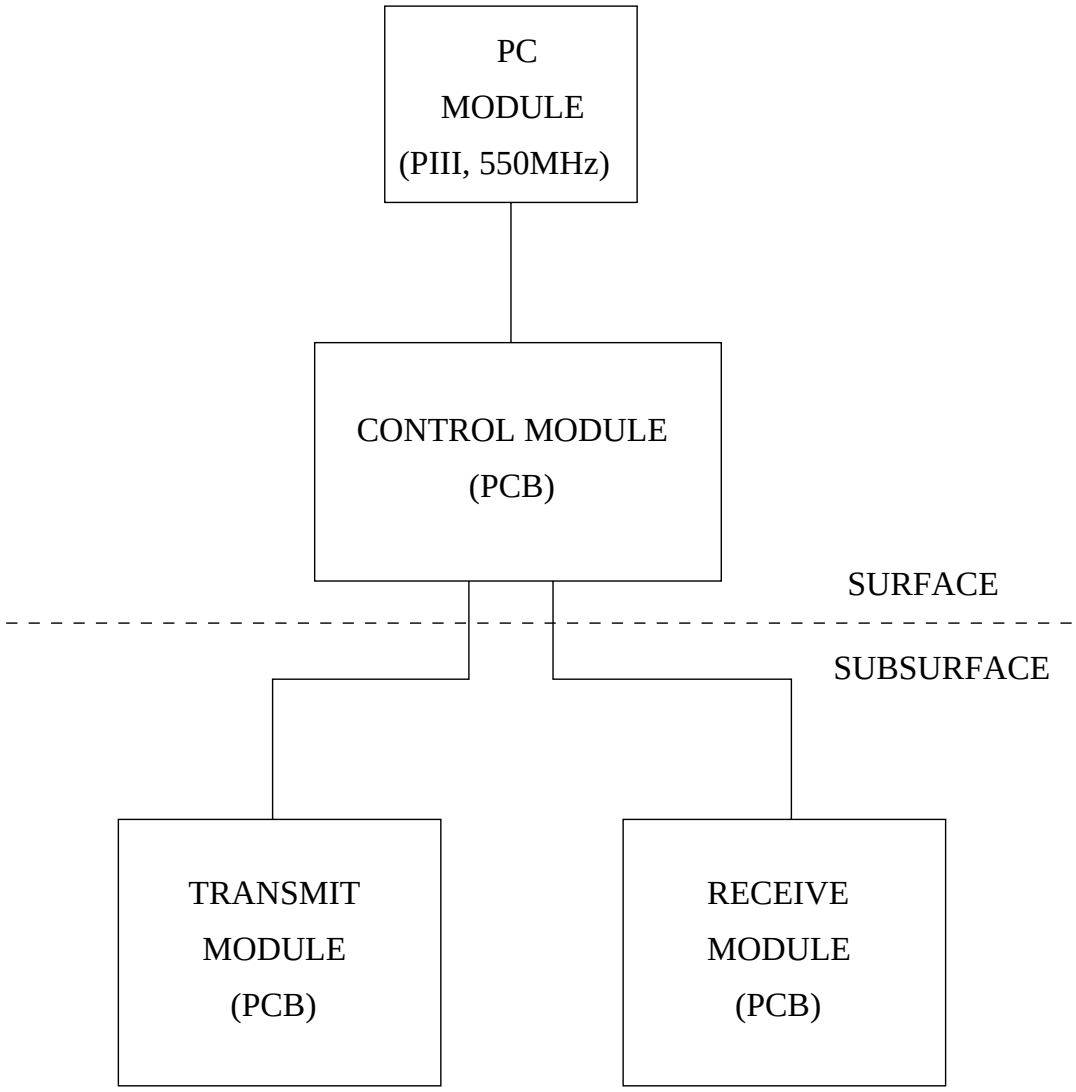

Figure 5.6: The Four Modules

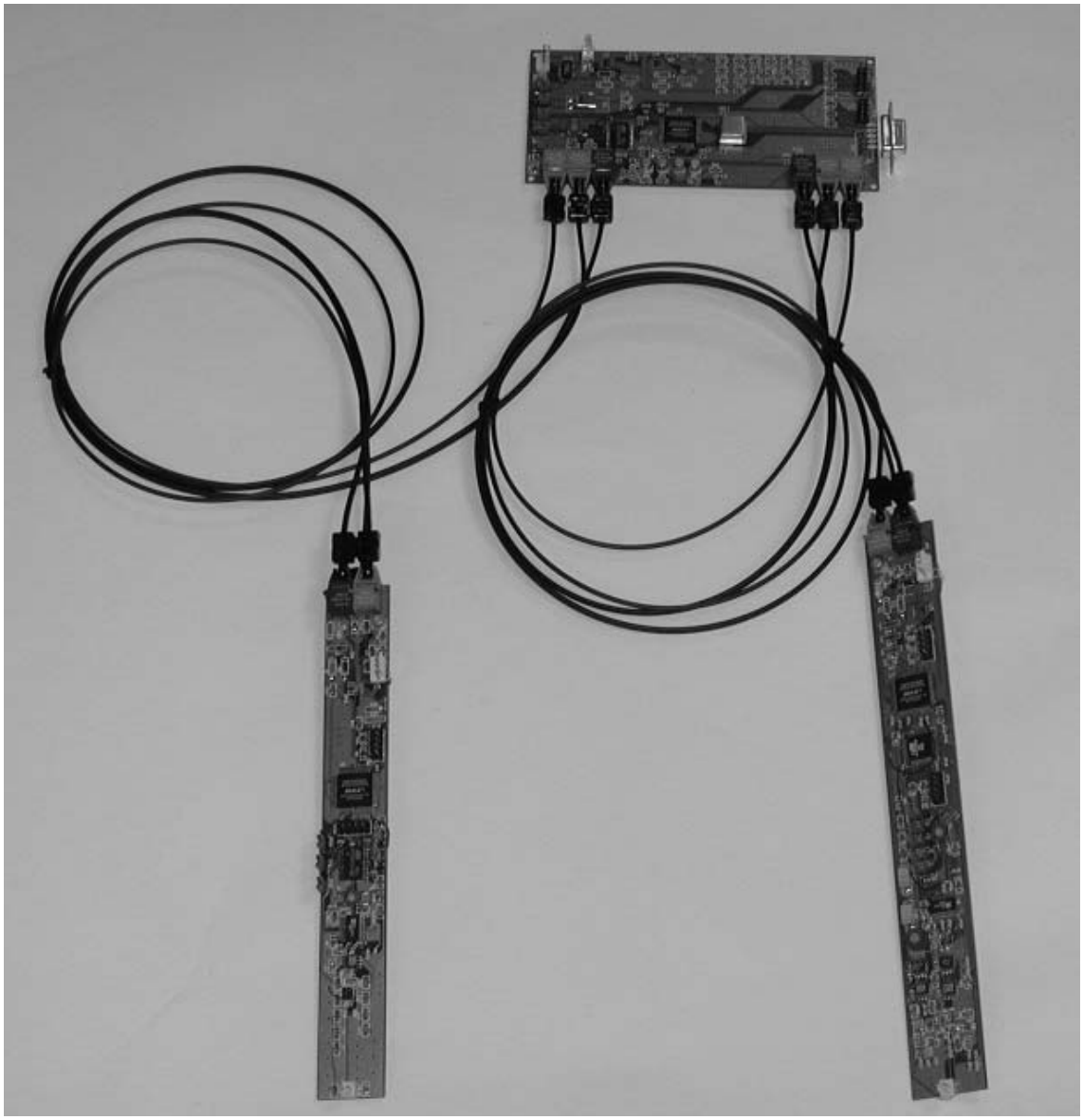

Figure 5.7: Final PCB Hardware System

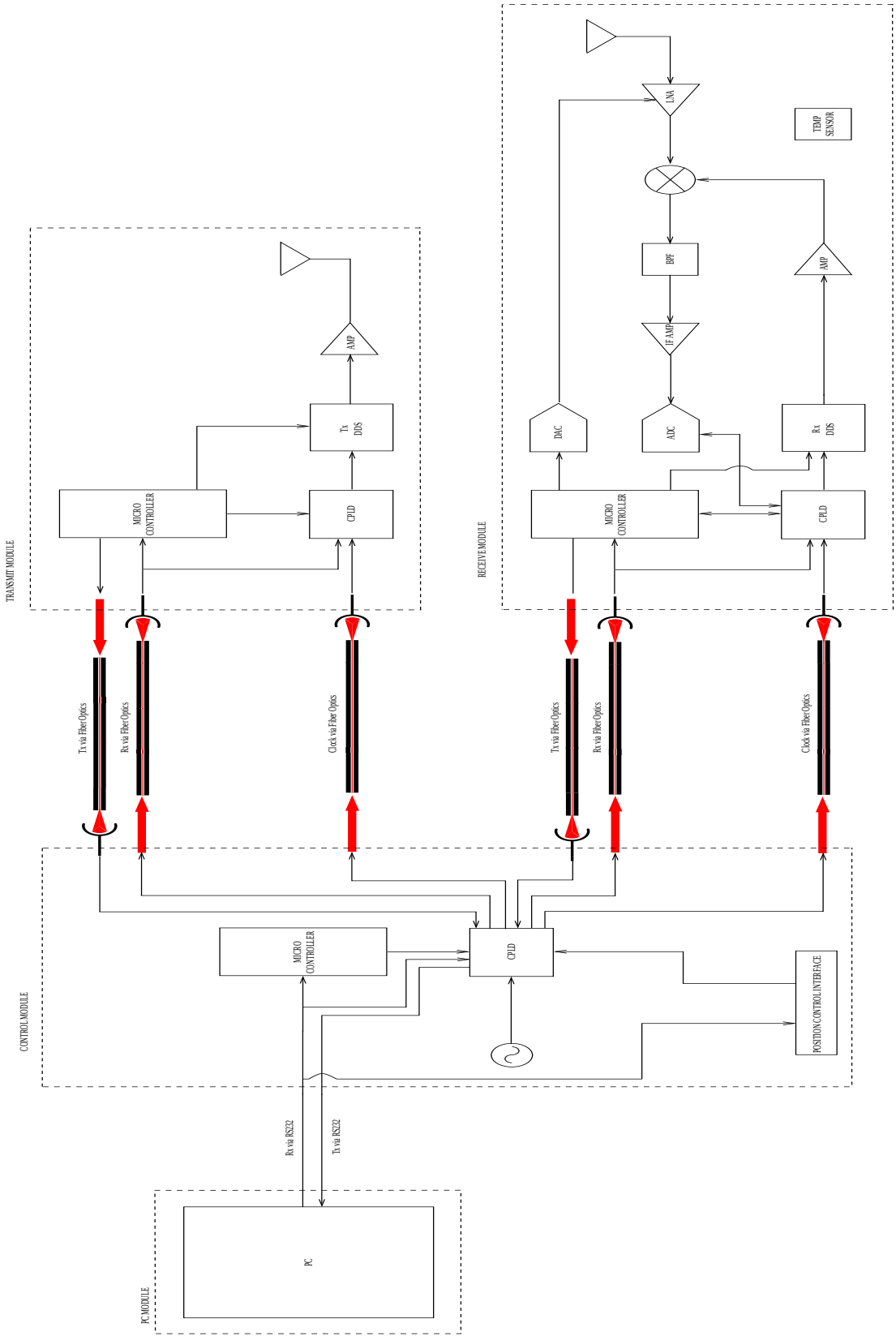

Figure 5.8: Four Modules with Components

sent synchronously to ensure the frequency update signal arrives simultaneously to both synthesisers [24, page 7].

The position control interface is used to determine the exact position of the Receive Module, and the Transmit Module within the borehole. This dissertation does not utilise the position control interface, but provision is made for future use.

The main function of the microcontroller (AT90S2313) is to control the multiplexer logic implemented by the CPLD[33] [28, page 3-3]. The multiplexer logic enables the PC to listen to the Control Module, Positioner Interface, Transmit Module, or the Receive Module. Only one module is allowed to talk to the PC at a time to prevent line contention. In this dissertation only the Transmit, and the Receive Module will send messages to the PC.

The flow diagram in Figure C.1 shows the sequence of events in the embedded C source code[34]. On power up, the data storage buffer (**array**), and the output pins are initialised, the UART is enabled, and the baud rate for the UART is set at 2400bps[35]. The microcontroller then waits for seven bytes to arrive from the PC (**Receive_From_PC()**).

These seven bytes represent the protocol of the system. The first byte represents the address (source and destination), the second byte represents the identification packet identifier (represents an instruction for the microcontroller), and the remaining five bytes contain the data associated with the specific instruction. The remaining five bytes are not utilised in the Control Module. No error checking is performed on the protocol, and therefore, transmission error can occur. This should be considered for future applications[36].

These seven bytes are then stored in **array** after they have been received. The first byte, and the second byte are compared to the address of the control microcontroller (Source_Dest_Address_To_ControlUcont), and the various identification packet identifiers (ID_Packet_Identifier_TxMod and ID_Packet_Identifier_RxMod), respectively. The identification packet identifiers instruct the microcontroller as to which module should be allowed to talk to the PC. If there is a match then the select lines to the multiplexer are adjusted so that the module defined by the matched identification packet identifier can talk to the PC.

[33]File location on CD: D:\Firmware\Control\Control.gdf
[34]File location on CD: D:\Software\Control\main.c
[35]Refer to section 5.3.4.
[36]Refer to Chapter 7.

The microcontroller then waits for another seven bytes to arrive, and the process repeats itself.

5.4.2 Transmit Module

The Transmit Module consists of the following main components: DDS, CPLD, amplifier, and microcontroller, as shown in Figure 5.8. The schematic can be found in Figure A.2. The PCB can be found on the CD[37].

The DDS (AD9851), or direct digital synthesiser, generates the CW, sinusoidal, analogue signal frequencies required for transmitting, and is utilised due to being part of the user requirements statement[38] [24].

The CPLD (EPM7128STC100-15) implements a flip-flop, and a modulus 4 counter[39], which is used to synchronise the synthesiser frequency update signal (FQ_UD) with the Receive Module synthesiser frequency update signal in order to establish a coherent system[40]. The CPLD also acts as a buffer for the clock signal, as mentioned above [38].

The amplifier (AD8011) is used to amplify the output of the synthesiser to ± 1 volts, which sees a 51ohm load, as shown in the schematic [35]. This results in an average transmit power: $P_{av} = \frac{v_{rms}^2}{R} = \frac{1}{2 \cdot 51} = 9.9dBm$, which is close to the specified $10dBm$ mentioned in the user requirements statement[41] [18, page 8].

The main function of the microcontroller (AT90S2313) is to program the synthesisers with the required frequency/phase word [28, page 3-3], [24, page 8, and 12]. It also resets the synthesiser, which is important for system coherency, as mentioned in section 5.5. The microcontroller also enables/disables the flip-flop implemented by the CPLD, and sends a message to the PC indicating that the frequency update was successful.

The flow diagram in Figure C.2 shows the sequence of events in the embedded C source code[42]. On power up, the same sequence of events that takes place in the Control Module power up sequence occurs here, except a new storage buffer (**Update_Successful**) is also initialised. The protocol remains the same as above,

[37] File location on CD: D:\Hardware\Transmit\PCB\Transmit.pdf
[38] Refer to section 1.1.
[39] File location on CD: D:\Firmware\Transmit\transmit.gdf
[40] Refer to section 5.5.
[41] Refer to section 1.1.
[42] File location on CD: D:\Software\Transmit\main.c

except the remaining five bytes are utilised, and they represent the frequency/phase update word. The microcontroller waits for seven bytes to arrive from the PC, and stores them in **array** (**Receive_From_PC()**).

The first byte, and the second byte are compared to the address of the transmit synthesiser (Source_Dest_Address_To_Synthesizer), and the identification packet identifier that instructs the microcontroller to program the synthesiser with the frequency/phase word (ID_Packet_Identifier_Frequency_Word), respectively. If there is a match, then the next four bytes in **array** are converted into one long int, which represents the 32 bit frequency word (**Bytes_To_Int()**) [24, page 12]. The DDS is then serially programmed with this 32 bit word, and the fifth byte, which represents the transmit phase (**Synthesiser()**) [24, page 12].

If no match occurs, then the first, and second byte are compared to Source_Dest_Address_To_Synthesizer, and the identification packet identifier that instructs the microcontroller to reset the synthesiser (ID_Packet_Identifier_Reset_DDS), respectively. If a match occurs, then the synthesiser is reset (**Reset_The_DDS()**), and then placed in serial programming mode, since the reset places the sythesiser in parallel programming mode (**Enable_SerialWord_DDS()**) [24, page 11].

If no match occurs, then the first, and second byte are compared to Source_Dest_Address_To_Synthesizer, and the identification packet identifier that instructs the microcontroller to flush out the residual data of the synthesiser (ID_Packet_Identifier_Flush_Data), respectively. If a match occurs, then the residual data is flushed with a zero frequency word in order to prevent the synthesiser from entering the factory test mode (**Flush_Residual_Data()**) [24, page 9]. This dissertation does not utilise this function, but provision has been made for it.

If no match occurs, then the first, and second byte are compared to the synthesisers broadcast address (Source_Dest_Address_To_Synthesizers), and the identification packet identifier that instructs the microcontroller to set the flip-flop within the CPLD (ID_Packet_Identifier_Set_Flip_Flop), respectively. If a match occurs, then the flip-flop is enabled in order to prepare for the frequency update signal (FQ_UD)[24, page 12].

If no match occurs, then the first, and second byte are compared to Source_Dest_Address_To_Synthesizers, and the identification packet identifier to find out if the frequency update signal was successful (ID_Packet_Identifier_Freq_Update_Sent), respectively. If a match occurs, then the flip-flop is disabled to ensure the frequency update signal to the synthesiser is disabled [24, page 12]. A message

(ID_Packet_Identifier_Frequency_Success_Update) is then sent to the PC to indicate that the update was successful (**Transmit_To_PC()**).

The microcontroller then waits for another seven bytes to arrive from the PC, and the process repeats itself.

5.4.3 Receive Module

The Receive Module consists of the following main components: DDS, CPLD, LNA, IF amplifier, DAC, BPF, ADC, temperature sensor, and microcontroller, as shown in Figure 5.8. The schematic can be found in Figure A.3. The PCB can be found on the CD[43]. The Receive Module utilises the heterodyne architecture mentioned in section 5.2.3.

The DDS (AD9851) generates the CW, analogue signal frequencies required for the local oscillator (LO), and is utilised due to being part of the user requirements statement[44] [24].

The CPLD (EPM7128STC100-15) implements a flip-flop, and a modulus 4 counter[45], which is used to synchronise the synthesiser frequency update signal (FQ_UD) with the Transmit Module synthesiser frequency update signal, in order to establish a coherent system[46] [38]. The CPLD's modulus 4 counter is also used for referencing the sampling, as mentioned in section 5.5. The CPLD contains an 80 bit shift register, which is used to store 5 x 12 bit sample values, and overhead from the ADC [27]. The first sample value is ignored, because there is a slight delay in the CONV signal from the CPLD to the ADC on the first sample [27, page 8, and 17]. The CPLD also divides down the master clock frequency to the sampling clock frequency, and distributes these clock signals to the ADC, and DDS[47] .

The LNA (AD603) provides a maximum of 40dB gain to amplify the input signal within the full-scale range of the ADC, as mentioned in section 4.5, and 5.3 [26]. However, due to the mixer's (RMS-1) RF input specifications only allowing a maximum input power of +1dBm, it is highly likely that 40dB of LNA gain can exceed this maximum RF input power rating causing the mixer to fail [36, page 56]. Therefore, an IF amplifier stage (AD8005) with a variable maximum gain of 500 is

[43]File location on CD: D:\Hardware\Receive\PCB\Receive.pdf
[44]Refer to section 1.1.
[45]File location on CD: D:\Firmware\Receive\receive.gdf
[46]Refer to section 5.5.
[47]Refer to section 5.3.4.

utilised, so that the signal ($\leq +1dBm$) proceeding the BPF can be amplified to fall within the full-scale range of the ADC [42].

The DAC (LTC1446L) is used to adjust the gain of the LNA from 0dB to 40dB, as mentioned in section 5.3 [41]. The BPF (CFWC455CZ) is used to filter through the required IF frequency, as mentioned in section 5.3 [25]. The ADC (LTC1404) is used to sample the IF signal [27].

A temperature sensor (LTC1392) has been provided for, but is not utilised in this dissertation [37]. The temperature sensor should be considered for future applications, because it is used to calibrate the sampling values that can vary due to temperature[48].

The microcontroller (AT90S8515) peforms the same functions as the Transmit Module's microcontroller mentioned above, but also performs two additional functions: sends signal to start the sampling, and programs the DAC which sets the gain of the LNA [28, page 6-3].

The flow diagram in Figure C.3 shows the sequence of events in the embedded C source code[49]. The sequence of events is the same as the sequence of events in the Transmit Module above, except the address is now Source_Dest_Address_To_Synthesizer2, and on power up, an additional two data storage buffers are initialised: **sample**, and **Byte**. The sample buffer (**sample**) stores the ADC samples as ints, and the byte buffer (**Byte**) stores these ints as bytes (4 MSB, and 4 LSB), so that they can be sent to the PC.

An additional two comparisons are done: the first, and second byte are compared to Source_Dest_Address_To_Synthesizer2, and the identification packet identifier which instructs the microcontroller to initiate the sampling process (ID_Packet_Identifier_ADC_Sample_Start), respectively. If there is a match, a signal is sent to the CPLD to initiate the sampling process, mentioned in section 4.7 [27, page 17]. The microcontroller waits until the shift register is full (waits until the output of the shift register is high), and then stops the sampling process (**sample_set()**). The five samples are then clocked out of the shift register, and stored in **sample** (**capture_samples()**). The four out of the five samples are converted from ints to bytes, and stored in **Byte** as four most significant bytes, and four least significant bytes (**int_to_two_bytes()**). This byte array (**Byte**) is then sent to the PC (**Tx_Samples_To_PC()**).

[48] Information supplied by Dr. Alan Langman.
[49] File location on CD: D:\Software\Receive\main3.c

If no match occurs, the first, and second byte are compared to the address of the synthesizer (Source_Dest_Address_To_Synthesizer2), and the identification packet identifier, which instructs the microcontroller to program the DAC to adjust the gain of the LNA (ID_Packet_Identifier_Gain_Control), respectively. If there is a match, then the DAC is loaded with the required 12 bit user defined gain word, and updated (**gain_control()**) [26, page 5], [41].

The microcontroller then waits for another seven bytes from the PC, and the whole process repeats itself.

5.4.4 PC Module

The PC Module utilised is a COTS, Pentium III, 550MHz, standard PC, as shown in Figure 5.6, and 5.8. This PC runs the Windows 95 platform. In the field, a lap-top should be used due to its ease of portability, and light weight. However, in this dissertation, the system will not be utilised in the field, and therefore a standard PC is suffice[50]. Any platform can be utilised so long as it supports a windows environment, and contains a Java interpreter in order to run a Java Swing application[51], which forms the graphical user interface (GUI) in this dissertation. The GUI allows the user to perform the following functions:

1. **Frequency Update** button: enter in frequency, and transmit phase shift then press button to perform frequency, and phase updating.
2. **Reset DDS** button: press button to reset synthesisers.
3. **Sample** button: press button to initiate the sampling process.
4. **LNA Gain** button: enter in gain, and press button to set the gain of the LNA.
5. **Power Up Reset** button: press button to reset the serial port members after power up.

These functions must always be performed in the following sequence after power up: 5, 2, 4, 1, and 3. Thereafter, only the functions 4, 1, and 3 need to be utilised.

[50] Refer to section 5.3.

[51] File location on CD: D:\Software\PC\SwingApplication.java

Each of these functions are explained by means of the flow diagrams in Figure C.4, and in Figure C.5. Figure C.4 represents the flow diagram of the GUI functions, and Figure C.5 represents the flow diagram of the Serial Port Event Listener[52], which receives the sample values from the Receive Module, and update successful messages from the Transmit, and Receive Modules, as mentioned in section 5.4.2, and 5.4.3. The protocol remains the same, as mentioned in section 5.4.1. In Figure C.4, all the GUI functions have action listeners[53] attached to their buttons (**addActionListener()**). Once the button is pressed an action is performed, and the rest of the loop is executed (**actionPerformed() = yes**), otherwise the loop is not executed (**actionPerformed() = no**).

If the **Frequency Update** button is pressed, a comparison is done on the user input transmit frequency to make sure it is within the specified frequency range[54], and a comparison is done on the user input transmit phase shift to make sure it is within the 0 to 360 degree range. If the comparison is confirmed, then the input transmit frequency, clock frequency, and transmit phase shift is stored in the object members **datacollect.outputfrequency**, **datacollect.inputclockfrequency**, and **datacollect.phaseshift**, respectively. The same is done for the local oscillator, except it only stores its frequency, and clock frequency in the object members **datacollect4.outputfrequency** and **datacollect4.inputclockfrequency**, respectively. The local oscillator frequency is offset from the transmit frequency by the IF, and the clock frequency is set to the master clock frequency[55].

The 32 bit frequency word, and the 5 bit transmit shift word which is used to program the synthesisers, is calculated for both the transmit synthesiser (**datacollect.phaseword()**, **datacollect.phaseshift()**), and the local oscillator synthesiser (**datacollect4.phaseword()**) [24, page 8]. These frequency, and transmit phase shift words are then converted into five bytes for transmission to the Transmit Module (**datacollect2.fourbyteword()**), and the Receive Module (**datacollect5.fourbyteword()**).

The serial port parameters are then set up to prepare for transmission (**datacollect3.setupserialport()**). The frequency word is then sent to both the Transmit, and Receive Module (**datacollect3.transmitport()**). A delay is added throughout the transmission process to ensure that the message arrives before the next message is

[52]File location on CD: D:\Software\PC\AccessingSerialPort.java
[53]Refer to any Java site for more information, e.g., http://java.sun.com/
[54]Refer to section 1.1.
[55]Refer to section 5.3.1, and 5.3.4.

sent. This is necessary, because no error checking is done[56]. A message is then sent to the Control Module to allow the PC to listen to the Transmit Module (protocol.ID_Packet_Identifier_TxMod). A message is then sent simultaneously to both the Transmit Module, and the Receive Module to prepare the flip-flops onboard the CPLDs for the frequency update signal (protocol.ID_Packet_Identifier_Set_Flip_-Flop). Finally, the frequency update signal is sent simultaneously to both the Transmit, and Receive Modules (protocol.ID_Packet_Identifier_Freq_Update_Sent) [24, page 12]. The process is now complete, and waits for the button to be pressed again.

However, in the meantime, the Transmit Module sends a message to the PC indicating the frequency update signal was successful. This process is explained using Figure C.5.

The Serial Port Event Listener waits until data has arrived at the serial port (**SerialPortEvent.DATA_AVAILABLE**). It then goes through an initialisation phase, and reads the data from the input stream into a buffer (**DataBuffer**). At the same time it returns the number of bytes read, and updates the static member, **TotalNumBytes**, with the total number of bytes read so far. If **TotalNumBytes** is equal to six, and **DataBuffer[1]** does not equal the identification packet identifer which tells the PC that four samples are stored in **DataBuffer** (protocol.ID_Packet_Identifier_Four_Samples_To_PC) it means that the the data received at the serial port must be a frequency update successful message from one of the synthesisers. A comparison is then done to find out whether the Transmit Module (protocol.Source_Dest_Address_From_Synthesizer), or the Receive Module (protocol.Source_Dest_Address_From_Synthesizer2) sent the message (protocol.ID_Packet_Identifier_Frequency_Success_Update).

If the message is from the Transmit Module then a "Update for board 1 was successful" message is displayed to the screen. A message is then sent to the Control Module to allow the PC to listen to the Receive Module (protocol.ID_Packet_Identifier_RxMod). A message is then sent to the Receive Module to find out if the frequency update signal was a success (protocol.ID_Packet_Identifier_Frequency_Success_Update). The Serial Port Event Listener then sets **TotalNumBytes**, and **offset** members to zero. It then waits for the Receive Module to reply that the frequency update was successful. The same sequence of events, as above, takes place, but this time the message is from the Receive Module (protocol.Source_Dest_Address_From_Synthesizer2). A "Update for board 2 was successful" message is displayed to the screen,

[56]Refer to section 5.4.1.

and the **TotalNumBytes**, and **offset** members are set to zero for next time round. Once again, the Serial Port Event Listener waits for data to arrive.

If the **Reset DDS** button is pressed, then a message is sent to both the Transmit, and the Receive Module, which results in the synthesisers being reset (protocol.ID_Packet_Identifier_Reset_DDS) [24, page 11]. The residual frequency word in the synthesisers also needs to be flushed out, since after reset a frequency update occurs to place the DDS in serial programming mode[57]. The synthesisers should be updated with a valid frequency/phase word as soon as reset occurs. This follows the same sequence of events as explained above.

If the **Sample** button is pressed, then the serial port parameters are set up (**datacollect3.setupserialport()**). A message is sent to the Control Module enabling the PC to listen to the Receive Module (protocol.ID_Packet_Identifier_RxMod). A delay is added, and then a message is sent to the Receive Module, which initiates the sampling (protocol.ID_Packet_Identifier_ADC_Sample_Start). This process is now complete, and waits for the button to be pressed again.

However, in the meantime, the Receive Module has finished sampling, and now sends the sample values back to the PC for processing. This process is explained using Figure C.5.

The initial same sequence of events mentioned above occurs, except this time ten bytes are sent to the Serial Port Event Listener, instead of six, because each of the four sample values has been divided into four most significant bytes, and four least signififcant bytes for transmission purposes. A comparison is done to see if the **TotalNumBytes** is equal to ten. If this is true, then a comparison is performed to make sure the message was sent by the receive Module, and the identification packet identifier, which tells the PC that four samples are located in **DataBuffer** (protocol.ID_Packet_Identifier_Four_Samples_To_PC). If a match occurs, then a "Sampling Successful" message is displayed to the screen.

The sample values are then stored in the object member **datacollect.sample**. These four sample values are then converted from bytes to shorts (**datacollect.bytes_to_short()**). Finally, the I, Q, phase, and amplitude values are calculated, and displayed to the screen (**datacollect.I_Q_Values()**)[58]. The **TotalNumBytes**, and **offset** members are set to zero, and the Serial Port Event Listener waits for data to arrive.

[57] Refer to section 5.4.2.
[58] Refer to section 4.7.

If the **LNA Gain** button is pressed, a comparison is performed to ensure that the user-defined gain is within the 0 to 40dB range, as mentioned in section 5.3.3. If this is true, the serial port parameters are set up (**datacollect2.setupserialport()**). The user-defined gain is then stored in the object member **datacollect.gain_value** as a float. This gain value is then used to determine the 12 bit word that the DAC needs to be programmed with, and this word is converted into two bytes (most signifcant, and least significant) to meet the transmission format requirements (**datacollect.DAC_Gain_Word()**) [26, page 5], [41]. This gain word is then sent to the Receive Module microcontroller, which programmes the DAC (**datacollect2.transmitport()**)[59]. A delay is added, and the process waits for the button to be pressed.

Finally, if the **Power Up Reset** button is pressed, the Serial Port Event Listener's **offset**, and **TotalNumBytes** members are set to zero (**datacollect2.PowerReset()**). This is important after power up, because pseudo data is sent to the serial port effecting these values, and hence, the operation of the software. The process then waits for the button to be pressed again.

5.5 Coherent Control

The system needs to be coherent in order to preserve the correct phase shift information[60]. The system's coherency is dependent on the reference clock signal[61]. The system coherency is established in the following manner, as shown in Figure 5.9:

5.5.1 Start Up Procedure

1. The reference divider is enabled at power-up, and divides down the reference clock frequency (REFCLK) to the required sampling frequency[62]. The reference clock to both synthesizers must be phase-locked with each other to ensure that the synthesizers are synchronous [24, page 7].

2. The synthesisers both need to be reset (RESET) at start up in order to place each synthesiser in the same phase, and state [24, page 5 and 11]. The RESET signal to each synthesiser does not have to be synchronous with each other.

[59] Refer to section 5.4.3.
[60] Information supplied by Dr Alan Langman.
[61] Information supplied by Prof. M.R. Inggs.
[62] Refer to section 5.3.

3. The modulus 4 counter is enabled at power-up. The modulus 4 counter is used as a reference to start the sampling, and the frequency updating [16, page 33]. This method will allow the receive phase to be preserved at any count number and at any time. This counter, once enabled, must not be reset. This will preserve the frequency to frequency coherency of the synthesizers.

5.5.2 Frequency Updating

This occurs by sending a common update signal (FQ_UD SIGNAL) to both phase continuous synthesizers [24, page 7]. The FQ_UD signal is synchronized with the reference clock, and the sample clock, as shown by the timing diagram at the top of Figure 5.9. The synchronization with the reference clock ensures that the synthesizer update delay remains uniform [24, page 3]. In order to ensure that the synthesisers remain frequency to frequency coherent it is important that the FQ_UD signal occurs when the synthesisers phase accumulators are always at the same point for each particular frequency step, because the synthesisers are phase continuous[63] [24, page 8]. Equation 5.5 shows this is achieved by synchronising the FQ_UD signal with the sample clock (count one of the modulus 4 counter).

$$y(nT) = \cos\left(2\pi \cdot f \cdot nT\right) \ (n = 0, 1, 2...\infty) \tag{5.5}$$

In equation 5.5, T represents the sampling clock period, n represents multiples of the sampling clock period, f represents the IF frequency, and $y\left(nT\right)$ represents the IF frequency amplitude values for multiples of the sampling clock period. In order for the above statement to be true, whenever the modulus 4 counter equals one then $y\left(nT\right)$ must always return the same value.

If $f = 455kHz$, and $T = \frac{1}{202.222kHz}$(inverse of sampling frequency) is substituted into equation 5.5, then $y\left(T\right) = 0$ volts, $y\left(5T\right) = 0$ volts, and so on. Therefore, the phase accumulators of the synthesisers will always be at the same point in time if synchronised with the sample clock, and hence the system will be frequency to frequency coherent.

It is also important for the system coherency that the synthesiser clock frequency is a multiple of the IF frequency. This will ensure that the phase error of the synthesisers

[63]Information supplied by David Brandon of Analog Devices.

is at a minimum, or within the 32 bits of resolution[64].

5.5.3 Sampling Process

At some point in time, the user of the system will wish to sample the signal by sending a signal to initialize the sampling (SAMPLE SIGNAL). The zero count detector, in Figure 5.9, starts the sampling (SAMPLE) on count zero and on the positive edge of the sampling clock (SAMPLE CLOCK), as shown by the timing diagram at the bottom of Figure 5.9. The system requires four samples for each step in frequency in order to extract the I, and Q values[65]. The system is fully coherent, since the user now knows the count number each sample will occur at.

The BPF should be allowed to settle before sampling takes place after each frequency step. The dwell time for each frequency step should be the inverse of the receiver bandwidth[66], which is $48\mu s$. The BPF settling time should be roughly around 5.208 times the dwell time, which is $250\mu s$[67]. The sampling should occur after this settling time for each frequency step.

5.6 Conclusion

In conclusion, the final design utilises the heterodyne architecture mainly because it does not experience the harmonic, or interference problems associated with the RF sampling, and homodyne architectures.

The choice of the frequency step size, and hence, transmit frequency is important in terms of the intermodulation products generated at the mixer output. The intermodulation products could end up in the IF band of interest if the transmit frequency is not chosen wisely.

There is no error checking performed on the software protocol, and hence, transmission error can occur. This could be a problem if a faster PC is utilised.

The synthesisers will remain frequency to frequency coherent if the frequency update signal occurs when their phase accumulators are always at the same point for each

[64]Information supplied by David Brandon of Analog Devices.
[65]Refer to section 4.7.
[66]Refer to section 5.3.2.
[67]Information supplied by Dr Alan Langman.

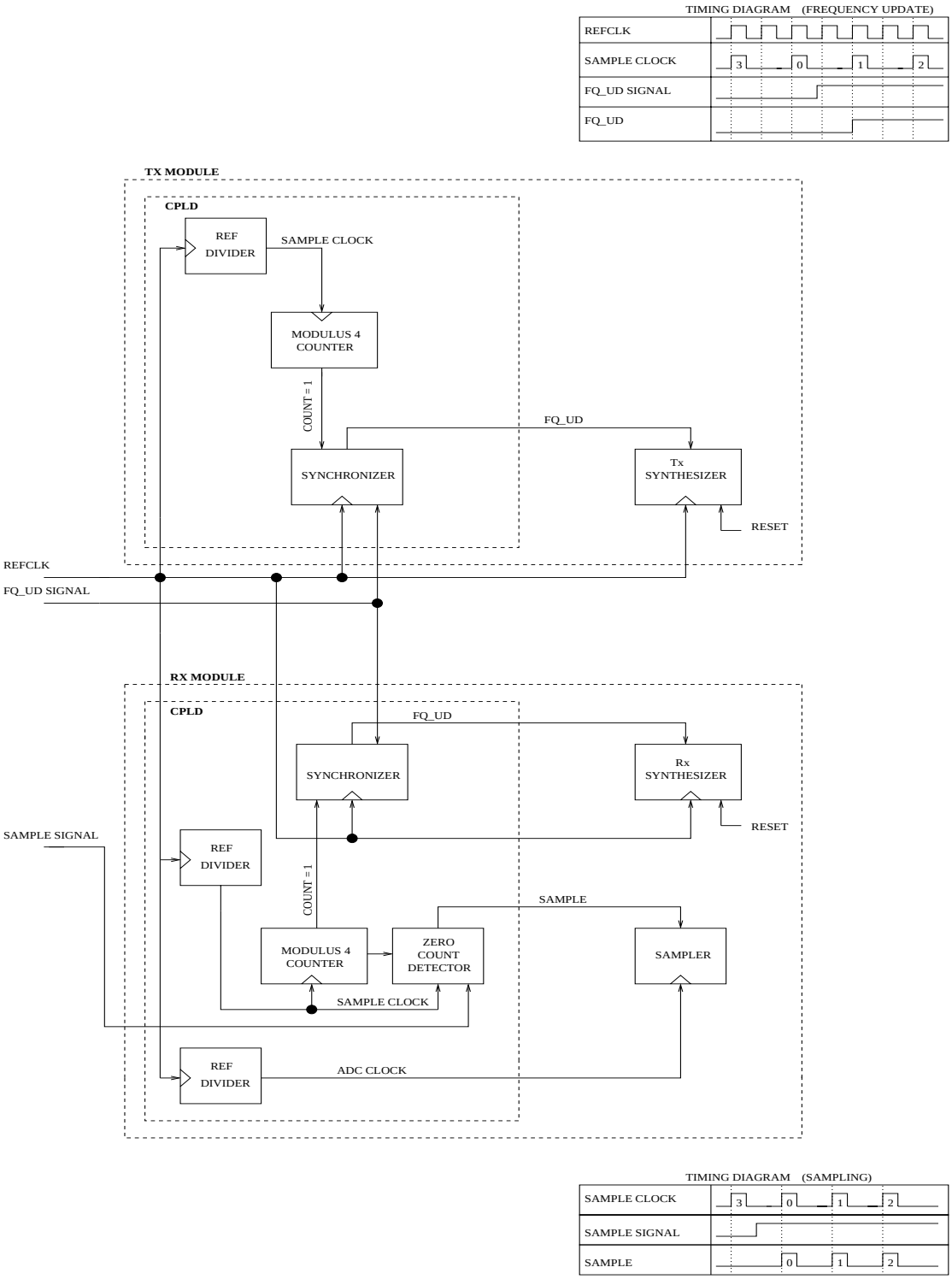

Figure 5.9: Coherent Control

particular frequency step. This is possible if the frequency update signal is synchronised with the sample clock. Hence, it is possible to get a frequency to frequency coherent system utilising the DDS technology.

Chapter 6

Design and Test Analysis

6.1 Introduction

This chapter involves the test analysis of the final design. The main system performance is measured, and compared with those specified in section 5.3. The following specifications are tested in this chapter: compression-free dynamic range, transmitter power, LNA Gain, BPF harmonics, and ADC harmonics. Finally, the overall system coherency is tested.

The transmitter power, and the LNA Gain are measured by means of a calibrated oscilloscope[1]. The receiver dynamic range, is measured by means of an oscilloscope, and a calibrated spectrum analyzer[2]. The BPF and ADC harmonics are measured with the same calibrated spectrum analyzer. Finally, the overall system coherency is tested with the PC User Interface Software mentioned in section 5.4.4.

The test setup is shown in Figure 6.1. Figure 6.1 excludes the power supply, PC Module, oscilloscope, and spectrum analyzer. Note, the setup consists of two new modules: the Attenuator Board (top of Figure 6.1), and the Power Board (bottom right of Figure 6.1). The Attenuator Board is used to step down the transmit signal amplitude, so that it falls within the LNA input range [26, page 2]. The Power Board distributes the power supplies +5V, -5V, and GND signals to the Control Module (bottom of Figure 6.1), Transmit Module (right of Figure 6.1), and Receive Module (left of Figure 6.1).

[1] Kikusui, 2 Channel, 100MHz Oscilloscope.
[2] Agilent E4404B, 9kHz-6.7GHz, Spectrum Analyzer.

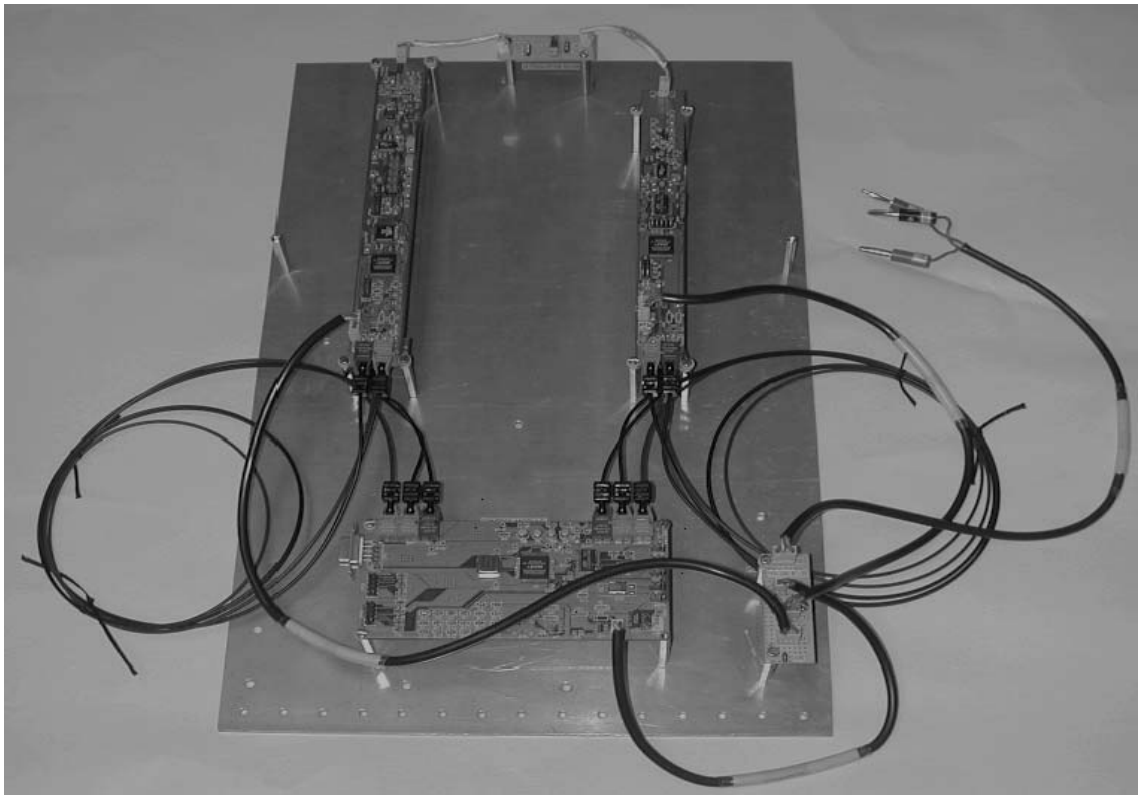

Figure 6.1: Test Setup

6.2 Receiver Dynamic Range

The receiver compression-free dynamic range is measured by placing an oscilloscope probe at the LNA output (JP9), and the LNA input (U9 pin 3), as shown in Figure A.3. The dynamic range requires two measurements: the 1dB compression point, and the noise power[3].

The 1dB compression point is measured by varying the potentiometer on the Attenuation Board to provide an input signal at U9 pin 3, so that the overall gain drops 1dB from its linear region [29, page 17.6]. The transmit frequency utilised for this test is 555kHz, and the LNA gain is set to 10dB. The 1dB compression point occurs when the peak input voltage is measured to be 140mV on the oscilloscope, which corresponds to -10.09dBm, because the input impedance of the LNA is 100 ohms [26, page 2]. This is close to the specified -11dBm in the LNA data sheet [26, page 2]. Therefore, the measured 1dB compression point is within system specifications.

The input noise power is measured by varying the potentiometer on the Attenuator Board, so that the input voltage amplitude of the LNA is measured to be 8mV peak

[3]Refer to section 5.3.7.

on the oscilloscope, which corresponds to -34.95dBm. The spectrum analyzer is then used to monitor the LNA input (U9 pin 3). The spectrum analyzer indicates that there is a 30.2dB difference between the input 8mV peak voltage amplitude, and the noise floor within the receiver bandwidth[4]. Note that this system is generally not a 50 ohm system, and therefore, the absolute power readings on the spectrum analyzer will be inaccurate, but the relative dB ratio will be accurate. Therefore, the noise power is measured to be at $-34.95dBm - 30.2dB = -65.15dBm$. This is 56.81dB greater than the calculated -121.96dBm noise power in section 5.3.7. Clearly, this noise power is not within system specifications.

Further investigation shows that there appears to be coupling of the 58.24MHz synthesiser clock signal, and the 9.2MHz harmonic of the 4.608MHz microcontroller crystal frequency onto the input of the LNA[5]. The 58.24MHz clock signal appears to be sitting at -37.02dBm, and the 9.2MHz harmonic is sitting at -50.15dBm, which are 2.07dB, and 15.2dB away from the -34.95dBm input signal, respectively.

The measured compression-free dynamic range for the current system is measured to be $-10.09dBm + 65.15dBm = 55.06dB$, which is 55.9dB less than the ideal calculated 110.96dB value in section 5.3.7. The real compression-free dynamic range is expected to be less than 100dB[6]. The coupling of the clock signals is likely to lower this measured value, as mentioned in section 5.3.7. The compression-free dynamic range can be improved by eliminating these interfering signals, and by reducing the overall noise floor power[7]. The coupling can be eliminated, and the input noise floor power reduced by utilising proper RF PCB routing methods, and the introduction of a ground, and power plane in the future [47, page 455]. The PCB boards are currently double-sided, and auto-routed due to time constraints.

6.3 Transmitter Power

The transmitter power is measured by first placing a jumper across JP25, as shown in Figure A.2, and then using an oscilloscope to monitor the peak transmit voltage for the entire transmit frequency range on JP25[8]. The transmit antenna is designed to see a 51 ohm load, as shown in Figure A.2, and mentioned in section 5.4.2. The

[4]Refer to section 5.3.2.
[5]Refer to section 5.3.4.
[6]Refer to section 5.3.7.
[7]Refer to equation 5.1.
[8]Refer to section 5.3.2.

results of these measurements can be seen in Table 6.1.

Table 6.1: Measured Transmitter Power Values

Tx Frequency (MHz)	V_{JP25} (V)	Tx Power (dBm)
0.555	0.90	9.0
1.010	0.90	9.0
1.465	0.90	9.0
1.920	0.90	9.0
2.375	0.90	9.0
2.830	0.90	9.0
3.285	0.92	9.2
3.740	0.95	9.5
4.195	0.97	9.7
4.650	0.99	9.8
5.105	1.00	9.9

In Table 6.1, the lower transmit frequency range tends to provide a 9dBm transmit power, while the higher frequency range tends to provide 9.2dBm to 9.9dBm of transmit power, which is close to the user specified 10dBm transmit power[9]. Therefore, the transmit power for the entire transmit frequency range is approximately within the required 10dBm value (0.1dBm-1dBm deviation) .

6.4 LNA Gain

The LNA gain is measured by placing an oscilloscope probe at the output of the LNA (JP9), and at the input of the LNA (U9 pin 3), as shown in Figure A.3. The ratio of the LNA output peak voltage over the LNA input peak voltage will give the measured gain of the LNA [47, page 233]. The LNA gain is programmed with 10dB, 20dB, 30dB, and 40dB. This test utilises a transmit frequency of 555kHz. The programmed LNA gain must correspond to the LNA measured gain. The results of these measurements can be seen in Table 6.2.

Table 6.2 shows that the measured LNA gain corresponds to the programmed LNA gain. However, the output signal becomes distorted when the programmed gain is set to 40dB. This is probably due to the coupling of the clock signals mentioned above, and with proper layout techniques the full 40dB range of gain can be achieved without distortion occuring[10]. In any case, the system is able to provide up to 30dB

[9]Refer to section 1.1.
[10]Refer to section 6.2.

Table 6.2: LNA Gain Measured, and Programmed Values

Programmed Gain (dB)	LNA Input (mV)	LNA Output (mV)	Measured Gain (dB)
10	14	45	10.14
20	14	134	19.62
30	4	120	29.54
40	4	400	40.00

of gain without distortion, which is greater than the required 25.4dB gain mentioned in section 5.3.3. Therefore, the system is able to provide the required LNA gain in order to operate in the environmental conditions mentioned in section 4.5.

6.5 BPF and ADC Harmonics

The BPF and ADC harmonics are measured by placing the spectrum analyzer probe at the BPF output (JP13), and the ADC input (U15 pin 2), as shown in Figure A.3. The results of the BPF, and ADC harmonic measurements for a 555kHz transmit frequency can be seen in Figure 6.2, and Figure 6.3, respectively.

Figure 6.2 shows that there is coupling of the 9.707MHz system clock signal, and the 4.608MHz microcontroller crystal clock, with its 9.2MHz harmonic, onto the BPF output[11]. The 9.707MHz, 4.608MHz, and 9.2MHz signals are 22dB, 25dB, and 18dB lower than the 455kHz IF signal, respectively. Not shown in Figure 6.2, is the coupling of the 58.24MHz synthesiser clock signal[12]. This 58.24MHz clock signal is 10dB lower than the IF signal. There also appears to be local oscillator feedthrough out of the BPF situated at 1.01MHz. The local oscillator signal sits 24dB lower than the IF signal.

Figure 6.3 shows that there is again coupling of all of the above mentioned signals, as well as, the local oscillator feedthrough on the ADC input. However, after the output BPF signal has gone through the IF amplifier, and then the low pass filter, as shown in Figure A.3, there is a considerable improvement in the suppression of the coupling. The 9.707MHz, 4.608MHz, and 9.2MHz signals are now 45.5dB, 49.5dB, and 44.5dB lower than the required IF signal at the ADC input. The 58.24MHz clock signal is now 41.5dB lower than the IF signal, although this is not shown

[11]Refer to section 5.3.4.
[12]Refer to section 5.3.4.

in Figure 6.3. The local oscillator feedthrough suppression has improved slightly (4.5dB), it is now 28.5dB lower than the required IF signal. Monitoring the ADC input (U15 pin 2) with an oscilloscope probe shows a fairly clean IF signal for the entire transmit frequency range used in Table 6.1.

The coupling of these clock signals can be eliminated by using the techniques mentioned above in section 6.2. The local oscillator is being fed through, because the output signal of the mixer is relatively small ($\leq -6dBm$) in amplitude that the BPF (optimum input $\geq 0dBm$) has no effect [25, page 6], [36, page 56]. If the mixer output signal is first amplified to a sufficient magnitude ($\geq 0dBm$), then the BPF will attenuate the local oscillator feedthrough sufficiently [25, page 6]. This can be achieved by placing the IF amplifier stage after the mixer, and then the BPF stage.

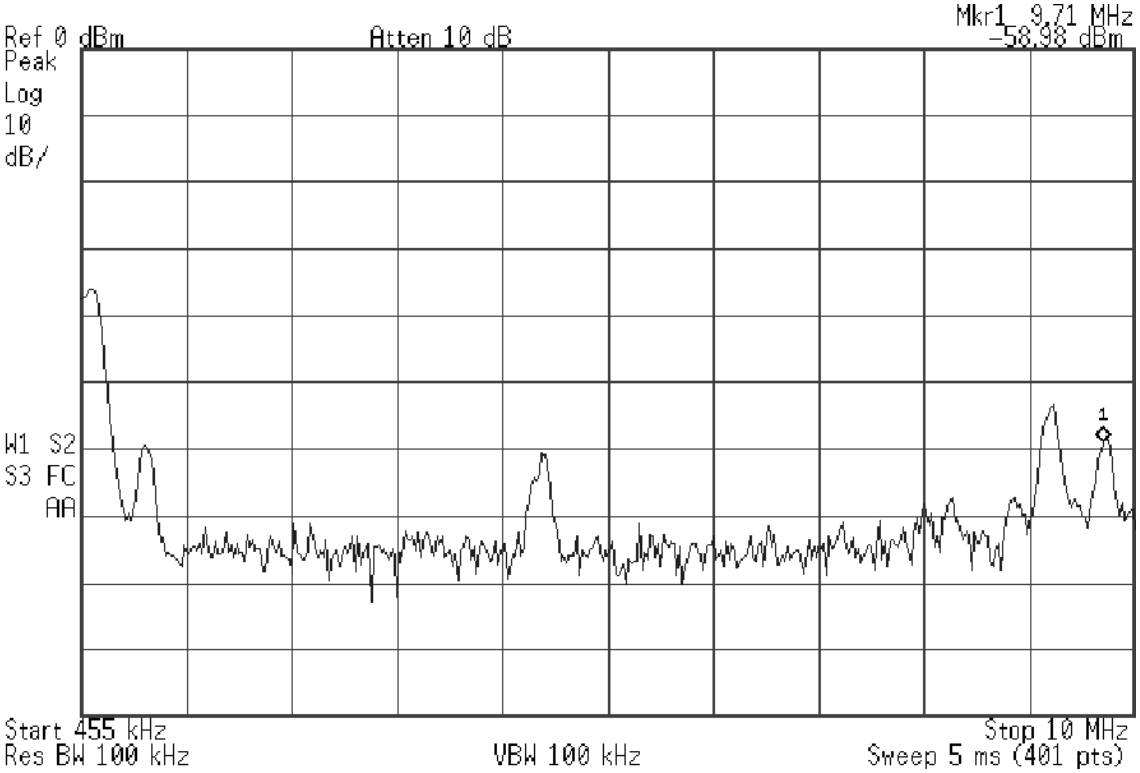

Figure 6.2: Output BPF Harmonics

6.6 System Coherency

The frequency to frequency coherency is tested for the entire transmit frequency range by using the PC user inteface software mentioned in section 5.4.4. The test involves taking ten phase samples with a zero degree transmit phase shift, and

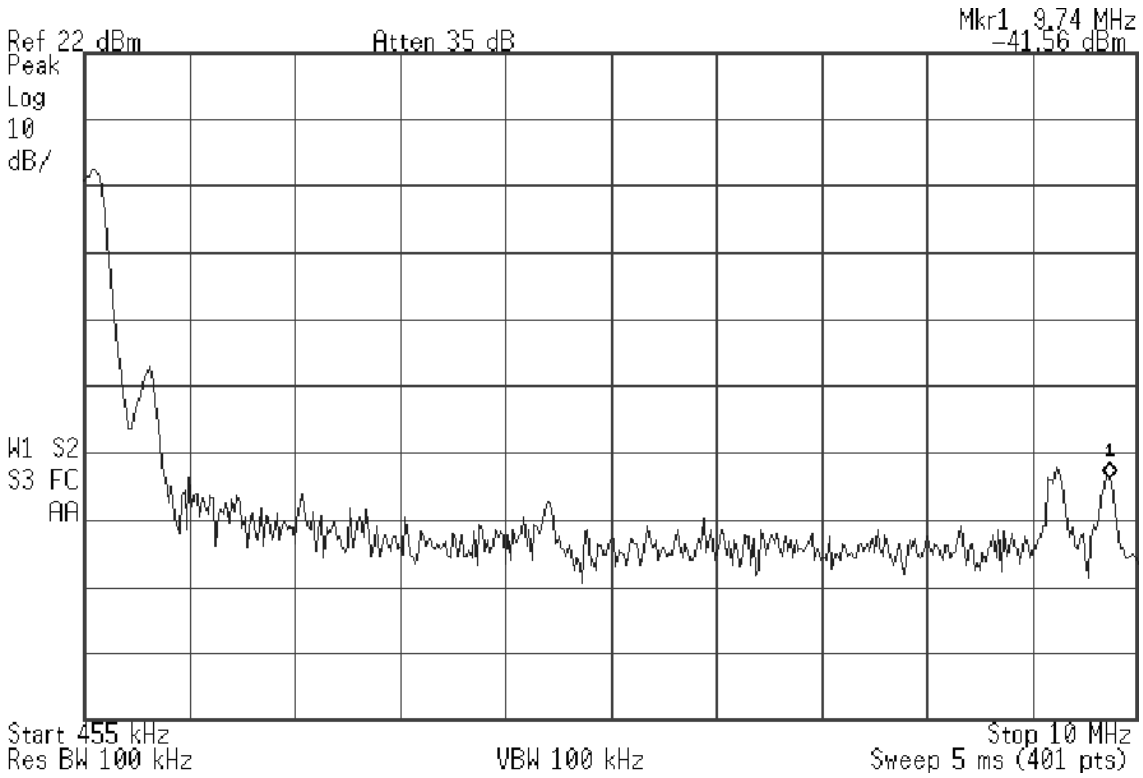

Figure 6.3: Input ADC Harmonics

then another ten phase samples with a ninety degree transmit phase shift for each transmit frequency. This cycle of events is repeated twice to test the system's frequency to frequency coherency. The phase samples (random variables) tends to approach a gaussian distribution as the overall number of phase samples becomes large, as proven by the Central Limit Theorem [48, page 482]. The test results are shown in Table 6.3.

In Table 6.3, μ_1, and μ_2 represents the mean value (in degrees) of the ten samples for cycle 1, and cycle 2, respectively. The σ_1, and σ_2 represent the standard deviation (in degrees) of the ten samples for cycle 1, and cycle 2, respectively. Finally, $\triangle\theta_1$, and $\triangle\theta_2$ represents the mean change in phase for cycle 1, and cycle 2, respectively. In Table 6.3, it is clear to see that by injecting a positive 90 degree transmit phase shift into the system results in a approximate negative 90 degree, or positive 270 degree change in phase. This is because the mixer creates the IF signal by subtracting the transmit signal frequency, and phase from the local oscillator signal frequency, and phase, as shown in Table 5.2. All that is needed to extract the true phase shift information is to negate the extracted phase shift information in Table 6.3. Table 6.3 shows that the system is frequency to frequency coherent for the entire frequency range, but is the change in phase accuracy accurate enough in order to reconstruct

the velocity map image without distortion, as mentioned in section 4.7.2?

In Chapter 4, section 4.7.2, it was shown that if the phase error is greater than 0.4 degrees then distortion of the reconstructed velocity map image tends to occur. In Table 6.3, the 1.465MHz, 2.375MHz, 3.285MHz, 4.65MHz, and 5.105MHz transmit frequencies all have a standard deviation for cycle 1, and cycle 2 of less than or equal to 0.4 degrees, and their overall change in phase for both cycles is therefore within the desired accuracy in order to produce a high quality reconstructed velocity map image[13]. However, for transmit frequencies 555kHz, 1.01MHz, 1.92MHz, 2.83MHz, and 3.74MHz, some of the standard deviations are greater than 0.4 degrees, and hence, the overall change in phase for both cycles will not always lie within the desired accuracy in order to produce a high quality reconstructed velocity map image. The exception to the rule seems to be the transmit frequency, 4.195MHz. This frequency has a standard deviation for cycle 1, and cycle 2 of less than 0.4 degrees, but the overall change in phase for both cycles is not within the desired accuracy mentioned above. The error is 0.72 for $\triangle\theta_1$, and 0.49 for $\triangle\theta_2$[14].

However, it should be noted that the use of a 12 bit ADC should yield a maximum phase error of approximately 0.027 degrees, as shown in section 4.7.2. The actual phase error is greater than this expected value, as mentioned above. This is probably due to poor PCB layout, and bypassing around the ADC, and the rest of the system as mentioned in section 6.2 [27, page 15]. It seems that poor supply bypassing, and routing loops can cause ADC errors [27, page 15]. It is a good idea to place the bypass capacitors as close as possible to the pins [27, page 15]. The introduction of a ground plane will eliminate, or reduce any potential difference in the grounds between the ADC, and the rest of the analogue circuitry, which appears as an error voltage in series with the ADC analog input signal [27, page 15]. Employing the above mentioned techniques should help improve the change in phase accuracy, and lead to a more efficient, and accurate coherent system.

Finally, the current system, as it stands, can improve the change in phase accuracy by increasing the overall number of samples taken in a process called coherent integration, as mentioned in section 4.3.

[13]Refer to section 4.7.2.
[14]Refer to Table 6.3.

Table 6.3: Frequency to Frequency Coherency Test Results

Tx Freq. (MHz)	$\mu_1, \sigma_1(0°)$	$\mu_1, \sigma_1(90°)$	$\mu_2, \sigma_2(0°)$	$\mu_2, \sigma_2(90°)$	$\triangle\theta_1(°)$	$\triangle\theta_2$ (°)
0.555	69.19, 0.80	-19.92, 0.41	70.15, 0.26	-19.28, 0.44	-89.11	-89.42
1.010	-57.33, 1.19	-147.33, 1.18	-56.64, 1.09	-147.41, 1.08	-90.00	-90.77
1.465	175.16, 0.34	85.31, 0.20	174.93, 0.27	85.04, 0.40	-89.86	-89.90
1.920	47.86, 0.70	-41.02, 0.75	47.80, 0.99	-42.16, 0.75	-88.88	-89.96
2.375	-78.82, 0.20	-169.14, 0.32	-79.00, 0.30	-169.16, 0.35	-90.32	-90.17
2.830	153.72, 0.54	63.94, 0.64	153.82, 0.40	64.30, 0.50	-89.79	-89.52
3.285	27.24, 0.17	-62.73, 0.23	27.51, 0.11	-62.25, 0.24	-89.96	-89.77
3.740	-97.79, 0.33	172.10, 0.36	-97.63, 0.34	171.79, 0.46	269.90	269.42
4.195	137.07, 0.27	47.79, 0.12	137.04, 0.22	47.53, 0.25	-89.28	-89.51
4.650	13.28, 0.29	-77.00, 0.30	13.78, 0.36	-76.14, 0.39	-90.29	-89.92
5.105	-111.85, 0.20	157.79, 0.22	-111.55, 0.16	158.10, 0.26	269.64	269.65

6.7 Conclusion

In conclusion, the test results have shown that there is coupling of clock signals near the LNA, BPF, and ADC due to inefficient PCB routing, and grounding. This is effecting the receiver compression-free dynamic range, and the LNA gain capability. However, the input to the ADC seems relatively uneffected by this coupling, and the maximum LNA gain is still within the required simulated gain value mentioned in section 4.5.

The mixer is experiencing local oscillator feedthrough that reaches the ADC input. This can be eliminated in the future by placing the IF amplifier after the mixer, and then the BPF after the IF amplifier. The measured transmit power corresponds to the transmit power specified in the user requirements statement mentioned in section 1.1.

The system is frequency to frequency coherent for the entire transmit frequency range, which satisfies the main aim of this dissertation. It appears that half of the transmit frequencies yield a phase error less than 0.4 degrees, and hence, will result in a high quality image reconstruction. The overall phase accuracy can be improved by utilising coherent integration.

Finally, the receiver compression-free dynamic range, LNA gain capability, phase accuracy. and overall system performance can be improved in the future by utilising efficient PCB routing techniques, power planes, and ground planes.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

Based on the findings in this dissertation, the following conclusions may be drawn:

The Physical Model of the Radon Transform can be derived by looking at the E-field of the EM wave, as proven through the mathematics in section 3.2.

The utilisation of the phase information yields a much more accurate image reconstruction than amplitude information, as proven with the Matlab simulation in section 4.7.2. The velocity map image reconstruction process utilises the phase information, and is able to handle an ADC with an 8 bit, or 12 bit resolution, which corresponds to utilising an ADC with a 47.78dB, and 67.78dB SNR, respectively[1]. However, the attenuation map image reconstruction process utilises the amplitude information, and is only able to handle an ADC with a 12 bit resolution, and hence, must utilise an ADC with a minimum SNR equal to 67.78dB. A 67.78dB SNR corresponds to a 0.027 degree phase error, and a 47.78dB SNR corresponds to a 0.3 degree phase error. Therefore, utilising the phase information reduces the resolution requirements of the ADC, because it allows for a greater degree of phase error than the amplitude information, as shown in section 4.7.2.

The heterodyne architecture is the system of choice, because the RF sampling, and homodyne architectures are more prone to harmonic interference, as mentioned in section 5.2.1, and section 5.2.2. The RF sampling architecture requires a BPF with a wide bandwidth in order to allow the 500kHz-5MHz transmit frequency to pass

[1]Refer to section 4.7.2.

through. This is a disadvantage, because interference from the outside can fall within this bandwidth, and mix with the receive signal, corrupting it [45, page 1]. The harmonics of the receive signal are not filtered out, and are also likely to mix with the receive signal, as mentioned in section 5.2.1. The homodyne architecture is a problem, because the harmonics are mixed down to baseband[2], and this can corrupt the required signal [16, page 18]. However, in the heterodyne architecture the harmonics tend to fall outside the IF bandwidth, provided the transmit frequencies, and BPF bandwidth are chosen correctly, as explained in section 5.2.3, and section 5.3.2.

No error checking is performed on the protocol used in the software for the Control Module, Transmit Module, Receive Module, and the PC Module, as mentioned in section 5.4.1. Therefore, error in data transmission can occur.

The system's compression-free dynamic range, LNA gain, BPF output, and ADC input are all being effected by the undesirable coupling of the clock signals[3]. The input of the LNA is experiencing coupling of the 58.24MHz synthesiser clock signal, and the 9.2MHz harmonic of the 4.608MHz microcontroller crystal frequency[4]. The 58.24MHz clock signal and the 9.2MHz harmonic are 2.07dB, and 15.2dB from the desired input signal, respectively. The LNA experiences distortion of the output signal when the gain is set to 40dB. The BPF output, and the ADC input all experience coupling of the above clock signals, as well as, the 9.707MHz system clock signal[5]. The coupling is being caused by improper routing of the RF PCB modules, and the fact that no power, or ground plane is being utilised [47, page 455]. The PCBs were auto-routed, and utilise two layers due to time-constraints.

The BPF output, and the ADC input are also experiencing local oscillator feedthrough, as mentioned in section 6.5. The local oscillator signal sits 24dB, and 28dB lower than the required IF signal at the BPF output, and the ADC input, respectively. The local oscillator is being fed through, because the output signal of the mixer is relatively small ($\leq -6dBm$) in amplitude that the BPF (optimum input $\geq 0dBm$) has no effect [25, page 6], [36, page 56].

The system is frequency to frequency coherent for the entire transmit frequency range, which satisfies the main aim of this dissertation[6]. A zero, and ninety degree

[2]Refer to Table 5.1.
[3]Refer to sections 6.2, 6.4, and 6.5.
[4]Refer to section 5.3.4.
[5]Refer to sections 5.3.4, and 6.5.
[6]Refer to section 6.6.

transmit phase was injected into the system, then ten phase samples were taken for each transmit phase over the entire transmit frequency range. This cycle was repeated twice. The mean, and standard deviation of these extracted ten phase samples were calculated, and appear in Table 6.3.

Table 6.3, clearly shows the change in phase ($\triangle\theta_1$, $\triangle\theta_2$) for the entire transmit frequency range to be approximately the desired negative 90 degrees, or positive 270 degrees. In Table 6.3, the 1.465MHz, 2.375MHz, 3.285MHz, 4.65MHz, and 5.105MHz transmit frequencies all have a standard deviation for cycle 1, and cycle 2 of less than or equal to 0.4 degrees, and their overall change in phase for both cycles is therefore within the desired accuracy in order to produce a high quality reconstructed velocity map image, as explained in section 4.7.2. However, the transmit frequencies 555kHz, 1.01MHz, 1.92MHz, 2.83MHz, and 3.74MHz, generally have standard deviations which are greater than 0.4 degrees, and hence, the overall change in phase for both cycles will not always lie within the desired accuracy in order to produce a high quality reconstructed velocity map image, as explained in section 4.7.2.

The 12 bit ADC is experiencing a phase error greater than the expected 0.027 degrees shown in section 4.7.2. This is probably due to poor PCB layout, and bypassing around the ADC, and the rest of the system as mentioned in section 6.2 [27, page 15].

Finally, the system satisfies all the requirements of the user requirements statement spelled out in section 1.1.

7.2 Recommendations

Based on the findings, and the conclusions in this dissertation, the following recommendations are made:

1. The software for the Control Module, Transmit Module, Receive Module, and the PC Module must incorporate error checking in the future to guarantee that the data message always arrives. This will ensure that if a faster PC is utilised, the software will not experience timing problems, and hence cause the system to fail. A good protocol to use is TCP, or transmission control protocol, because there is no error in transmission, due to TCP being a "connection-oriented" protocol [49, page 78].

2. The next version of this system must utilise proper RF PCB routing methods, and must incorporate a power, and ground plane [47, page 455]. This will help eliminate the coupling of the 58.24MHz synthesiser clock signal, and the 9.2MHz harmonic of the 4.608MHz microcontroller crystal frequency on the LNA input, BPF output, and ADC input [47, page 455]. It will also help to reduce the overall input noise floor power, and hence, improve the compression-free dynamic range[7]. The coupling of the 9.707MHz system clock present at the BPF output, and the ADC input will also be eliminated [47, page 455]. The removal of these coupled signal will allow the LNA to operate effectively within the full 40dB range of gain, as mentioned in section 6.4. The introduction of a ground plane will eliminate, or reduce any potential difference in the grounds between the ADC, and the rest of the analogue circuitry, which appears as an error voltage in series with the ADC analog input signal [27, page 15]. This will improve the overall change in phase accuracy. Employ sufficient supply bypassing, and avoid routing loops around the ADC, which can cause ADC errors [27, page 15]. The bypass capacitors must be placed as close as possible to the ADC pins [27, page 15].

3. The next version of this system must be restructured, so that the IF amplifier is placed after the mixer, and the BPF is placed after the IF amplifier. This will ensure the mixer output signal is first amplified to a sufficient magnitude ($\geq 0dBm$), which will allow the BPF to attenuate the undesirable local oscillator feedthrough sufficiently[8] [25, page 6].

4. The current system must utilise the coherent integration method in order to improve the change in phase accuracy, so that the error is less than or equal to 0.4 degrees[9] [18, page 144]. This will ensure that the velocity map image can be reconstructed without distortion occuring.

5. Finally, a fully-functional system that can be used in the field should be designed. This involves designing the transmit, and receive antenna. Special emphasis must be placed on the fibre optics involved, because the cables can become snagged, and break loose in the borehole.[10]

[7] Refer to equation 5.1.
[8] Refer to section 6.5.
[9] Refer to section 4.7.2, and 6.6.
[10] Information supplied by Prof. Iain Mason.

Bibliography

[1] Deans, SR, "The Radon Transform and Some of Its Applications", New York: John Wiley and Sons, Inc. , 1983.

[2] Mensa, DL, "High Resolution Radar Cross-Section Imaging", London: Artech House, Inc. , 1991.

[3] Dougherty, ME, Barker, DL, Wood, TR, and CF. Knutson, "An Evaluation of Borehole and Ground Penetrating Radar for Vadose Zone Characterization in Fractured Basalts", http://ladmac.lanl.gov/ mgls/95Sym/ Papers/ Dougherty

[4] Ramirez, A, and W. Daily, "Electrical Resistance Tomography for Subsurface Imaging", http://www-ep.es.llnl.gov/www-ep/esd/ert/ert.html

[5] Pihlman, M, and PE. Harben, "Low Frequency Electromagnetic Cross-Borehole Imaging", Lawrence Livermore National Laboratory, 1988.

[6] Slaney, M, Kak, AC, and L. Larsen, "Limitations of Imaging with First-Order Diffraction Tomography", IEEE Trans. On Microwave Theory and Techniques, Vol. MTT-32, No. 8, August 1984.

[7] Thomas, AL, "Cross Borehole Electromagnetic (EM) Imaging", http:// iridium.nttc.edu /env/tmp/002.html

[8] Lytle, RJ, and KA. Dines, "Iterative Ray Tracing Between Boreholes For Underground Image Reconstruction", Lawrence Livermore Laboratory, 1980.

[9] Ramirez, AL, Deadrick, FJ, and RJ. Lytle, "Cross-Borehole Fracture Mapping Using Electromagnetic Geotomography", Lawrence Livermore Laboratory, 1982.

[10] Borns, DJ, "Cross Borehole Electromagnetic (EM) Imaging", http:// www.pnl.gov/ WEBTECH/mwlid/emimag.html#desc

[11] Mason, I, "Tomography Software Help File", University of Sydney.

[12] Isaacson, AR, "Induction Sensing for Borehole Tomography", University of Cape Town, 1997.

[13] Noon, DA, "Stepped Frequency Radar Design and Signal Processing Enhances Ground Penetrating Radar Performance", University of Queensland, 1996.

[14] Stewart, J. "Calculus. 2nd ed.", California: Brooks/Cole Publishing Company, 1991.

[15] Ramo, S, Whinnery, JR, and T. Van Duzer. "Fields and Waves in Communication Electronics", New York: John Wiley and Sons, Inc., 1965.

[16] Farquharson, G. "Ground Penetrating Radar Design Document", University of Cape Town, 1998.

[17] Tattersfield, G. "Electromagnetic Field Theory", University of Cape Town, 1996.

[18] Hovanessian, S.A. "Radar System Design and Analysis", Norwood, MA: Artech House, 1984.

[19] Allison, D. "Matrix Methods for Engineers", University of Cape Town, 1995.

[20] Press, WH, Teukolsky, SA, Vetterling, WT, and Flannery, BP. "Numerical Recipes in C: The Art of Scientific Computing", Cambridge University Press, 1992.

[21] Oppenheim, AV, Schafer, RW. "Discrete-Time Signal Processing", New Jersey: Prentice -Hall Inc., 1989.

[22] Garcia, AL. "Probability, and Random Processes for Electrical Engineering", New York: Addison Wesley Publishing Co., 1994.

[23] Kingsley, S, and Quegan S. "Understanding Radar Systems", Mendham: SciTech Publishing Inc., 1999.

[24] Analog Devices, Inc., "AD9851 CMOS 180MHz DDS/DAC Synthesizer " Data Sheet, 1998.

[25] Murata, "Murata Products Search Engine CFWC455CZ" Data Sheet, 1998.

[26] Analog Devices, Inc., "AD603 Low Noise, 90MHz Variable-Gain Amplifier " Data Sheet, 1995.

[27] Linear Technology, "LTC1404 Complete SO-8, 12 Bit, 600ksps ADC with Shutdown" Data Sheet, 1998.

[28] Atmel, "AVR RISC Microcontroller Data Book", 1999.

[29] ARRL, "The ARRL Handbook for Radio Amateurs", 2000.

[30] Stremler, FG, "Introduction to Communication Systems, Third Edition", New York: Addison-Wesley Publishing Company, 1990.

[31] Coilcraft, "Surface Mount LC Filters" Data Sheet, 1999.

[32] STC, "JCO-Series: HCMOS-TTL Compatible Oscillator Type" Data Sheet, 1999.

[33] Linear Technology, "LT1381 Low Power 5V RS232 Dual Driver/Receiver with 0.1uF Capacitors" Data Sheet, 1993.

[34] Linear Technology, "LT1375/LT1376 1.5A, 500kHz Step-Down Switching Regulators" Data Sheet, 1995.

[35] Analog Devices, Inc., "AD8011 300MHz, 1mA Current Feedback Amplifier" Data Sheet, 1995.

[36] Mini-Circuits, "RF/IF Designer's Guide" Data Book, 1999.

[37] Linear Technology, "LTC1392 Micropower Temperature, Power Supply, and Differential Voltage Monitor" Data Sheet, 1995.

[38] Altera, "MAX 7000 Programmable Logic Device Family" Data Sheet, 1999.

[39] Hewlett Packard, "10 Megabaud Versatile Link Fiber Optic Transmitter and Receiver for 1mm POF and 200μm HCS" Data Sheet, 1994.

[40] Hewlett Packard, "Versatile Link: The Versatile Fiber Optic Connection" Data Sheet, 1998.

[41] Linear Technology, " LTC1446/LTC1446L Dual 12-Bit Rail-to-Rail Micropower DACs in SO-8" Data Sheet, 1996.

[42] Analog Devices, Inc., "AD8005, 270MHz, 400μA, Current Feedback Amplifier" Data Sheet, 1999.

[43] DARPA, "Digital Receiver Technology Program", http://www.darpa.mil/MTO/ADC/firstdemo.html

[44] Wepman, JA, and Hoffman, JR, "RF and IF Digitization in Radio Receivers: Theory, Concept, and Examples" NTIA Report 96-328, U.S. Department of Commerce, 1996.

[45] GCT Semiconductor, "Products Technology: Direct Conversion RF?", http://www.gctsemi.com/products/rf.asp

[46] Watson, RE., "The Communications Edge: Receiver Dynamic Range: Part 2", Tech Note, WJ Communications, Inc., 2001.

[47] Horowitz, P, and Winfield, H, "The Art of Electronics, 2nd Ed.", Cambridge: Cambridge University Press, 1989.

[48] Stremler, FG., "Introduction to Communication Systems, 3rd Ed.", New York: Addison-Wesley Publishing Company, 1990.

[49] Murhammer, M, Atakan, O, Bretz, S, Pugh, L, Suzuki, K, and Wood, D, "TCP/IP Tutorial and Technical Overview", Tech Report, IBM Corporation, 1998.

[50] Langman, A., "The Design of Hardware and Signal Processing for a Stepped Frequency Continuous Wave Ground Penetrating Radar", University of Cape Town, 2002.

[51] Jenkinson, M., "A Fast, Automated, N-Dimensional Phase Unwrapping Algorithm", Tech Report, University of Oxford, 2001.

Appendix A

Schematics

Appendix B

Matlab Simulation

Appendix C

Software Flow Diagrams