Theory, Design and Implementation of an IF Cancellation Module for use in a Stepped Frequency Continuous Wave Ground Penetrating Radar

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A dissertation submitted to the Department of Electrical Engineering,
University of Cape Town, in fulfilment of the requirements
for the degree of Master of Science in Engineering.

Cape Town, February 2004

Declaration

I declare that this dissertation is my own, unaided work. It is being submitted for the degree of Master of Science in Engineering in the University of Cape Town. It has not been submitted before for any degree or examination in any other university.

Signature of Author . . . . . .

Cape Town

23 February 2004

Abstract

A device has been designed that cancels the leakage signal between the transmit and receive antenna in a Stepped Frequency Continuous Wave Ground Penetrating Radar. The front end of the radar operates at high signal levels and, as a result, a large signal is coupled directly from the transmit to the receive antenna. This signal uses a significant part of the dynamic range of the data-capturing device, an analogue-to-digital converter (ADC). The objective of this cancellation is thus to increase the effective instantaneous dynamic range of the radar system.

Simulations show that 10-bit amplitude and phase resolution in the digital cancellation circuit would achieve maximum cancellation in the presence of phase noise and other sources of error. This result is confirmed when the hardware is tested.

The device was constructed and operates as intended. Tests show that cancellation exceeding 53dBm is possible through careful calibration. It was concluded that the device could successfully be integrated into the SFCW GPR and that it would achieve an increase in the instantaneous dynamic range.

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- My parents for their encouragement during the project, financial support and for proof-reading this document;
- My friends for providing a healthy balance between an academic career and a social life.

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List of Abbreviations

ADC Analog-to-Digital Converter

AM Amplitude Modulation

AQ Amplitude Quantization

CW Continuous Wave

DA Direct Analog

DAC Digital-to-Analog Converter

dBC/Hz Decibels below Carrier per Hertz

DDS Direct Digital Synthesizer

EMI Electro-Magnetic Interference

FFT Fast Fourier Transform

FM Frequency Modulation

FPGA Field Programmable Gate Array

IEEE Institute of Electrical and Electronics Engineers

IF Intermediate Frequency

IFC Intermediate Frequency Cancellation

LSB Least Significant Bit

LUT Lookup Table

LVDS Low-Voltage Differential Signalling

MSB Most Significant Bit

NCO Numerically Controlled Oscillator

NIST National Institute of Standards and Technology

PCB Printed Circuit Board

PDS Power Distribution System

PLD Programmable Logic Device

PLL Phase-Locked Loop

PM Phase Modulation

PT Phase Truncation

RF Radio Frequency

RMS Root Mean Square

ROM Read-Only Memory

Rx Receive

SFCW GPR Stepped Frequency Continuous Wave Ground Penetrating Radar

SFDR Spurious-Free Dynamic Range

SNR Signal-to-Noise Ratio

THD Total Harmonic Distortion

Tx Transmit

VGA Variable Gain Amplifier

Chapter 1

Introduction

This dissertation describes the theory, design and integration of an Intermediate Frequency Cancellation (IFC) module for use in a stepped frequency, continuous wave, ground penetrating radar (SFCW GPR). The objective of this cancellation device is to increase the overall instantaneous dynamic range of the radar system.

The front end of the ground penetrating radar system operates at high power levels. The high-powered transmit signal that directly couples into the receive antenna of the radar must be removed from the received data. This signal takes up a large portion of the dynamic range of the data-capturing device, a 16-bit analogue-to-digital converter (ADC). If this unwanted component could be cancelled out, the resultant signal could be amplified before it is sampled by the ADC. This would increase the instantaneous dynamic range of the system, since smaller targets will now be detectable and fewer radar scans are required to lift the signal above the system noise.

The method of cancellation makes use of a frequency generation technique known as Direct Digital Synthesis (DDS). DDS was chosen because it allows high resolution phase adjustment of the synthesized waveform, which will be shown to be of great importance in this application. The operation of the DDS technique will be outlined in this document, but for a rigorous treatment the reader is referred to Goldberg [24].

It will be seen that it is impossible to cancel the coupled signal perfectly. Various factors, such as uncorrelated phase noise in the transmit, receive and cancellation synthesizers and quantization errors in amplitude and phase of the DDS, are responsible for this. Imperfect calibration of the cancellation signal will also cause a deterioration in performance. The effects of the resulting partial cancellation are shown in this paper.

1.1 Objectives of Dissertation

The objectives of this dissertation can be summarized as follows:

1. To design hardware that will cancel the leakage signal from transmitter to receiver in a SFCW GPR radar, with the objective of increasing the instantaneous dynamic

range of the system.

2. To simulate the performance of this IF cancellation module, after a model of the system has been derived.

3. To measure the performance of the real system and compare it with the simulation results.

4. To draw conclusions as to the success of the concept of IF cancellation and its hardware implementation, as well as make recommendations for future work in this field.

1.2 Plan of Development

This document is organized as follows:

Chapter 1

The remainder of this introductory chapter will give the background to, and statement of, the problem at hand. The operation of SFCW-GPR will be explained first, since it is central to the problem. It will be shown that one of the shortcomings of Continuous Wave (CW) radars is the large signal coupled directly between the transmit and receive antennas of the radar. This leakage signal often dictates the dynamic range of the system, since it is larger in amplitude than the signals scattered back from targets.

The leakage signal contains no additional information about targets and can mask targets at close range or cause smaller targets to be undetectable by the data-capturing device (usually an ADC). It will be seen that one can remove this unwanted signal by subtracting a recreated version of the leakage signal from the returned signal. This can either happen in the RF stage or in the IF stage of the radar circuitry, depending on various factors. IF cancellation is more practical since only one frequency needs to be recreated, as opposed to many if cancellation is done in the RF stage of a SFCW radar.

Chapter 2

Chapter 2 presents the theory required to realize the IF Cancellation Module. Firstly, signal cancellation in the context of this paper is defined. It is shown that the most effective method of cancellation is adding two signals that are in exact anti-phase with respect to each other. Motivation for the use of Direct Digital Synthesis (DDS) will also be given.

The chapter then continues by explaining the operation of DDS. A breakdown of the system architecture will show that DDS has two main sources of error. Phase truncation and amplitude quantization produce spurious signals in the DDS output spectrum. The level of these spurs are dependent on the amplitude and phase resolution and a simulation

will show that there is no significant gain in signal-to-noise ratio when one has more resolution in one than the other. This result is an important one and is used in the hardware design phase.

The next part in the chapter deals with phase noise in signal sources and oscillators. An ideal oscillator exhibits a perfect spike at its output frequency in the frequency domain. All real oscillators exhibit phase noise, however, and this causes a spectrum that is not infinitely narrow. Phase noise and its causes are discussed as a measure of frequency stability in the frequency domain. The time domain version of frequency stability, jitter, is also explained and it will be shown how to convert from a phase noise plot to a jitter figure. This conversion is essential, since it is used in the simulation of the IF Cancellation Module. Allan Variance, another measure of frequency stability is also documented for completeness.

The chapter concludes by showing the effects of phase noise and amplitude and phase discrepancies in the SFCW radar by means of simulation. The simulation software was developed by Langman [40] during his PhD thesis. The simulation will show radar range-profiles and show how the performance deteriorates as phase noise, amplitude and phase errors are introduced in the various components in the system. Note that these are qualitative rather than quantitative simulations, the objective being to show the effect visually instead of mathematically.

Chapter 3

In Chapter 3, a model for the IF Cancellation Module is developed. The objective of the model is to create a simulation of the system which will show the effects of phase noise, quantization in the DDS and phase offsets on the IF signal.

The model includes the RF stage of the radar system. The transmitted signal is mixed with a receive signal and bandpass filtered to produce the system IF. The transmit and receive signals both contain phase noise, but the noise is largely correlated.

The cancellation signal is then generated, using exactly the same architecture as a real DDS would. The quantized DDS signal is filtered and added to the IF. The simulation shows the effects of phase noise in both the IF and the cancellation signal at various bit resolutions for the DDS. An important result is that there is no improvement in cancellation at relatively high levels of phase noise if the DDS resolution is increased.

The main shortcoming in the simulation is the IF bandpass filter. This could not be modelled completely, since the MatLab filters are difficult to edit. After some experimentation, the results seem promising, however.

Chapter 4

Chapter 4 contains a description of the hardware design process. The details will be kept to functional block-level, but should give the reader a good insight into what would be

required to reproduce such a cancellation module. Detailed circuit diagrams are contained on the included compact disc named Appendix B.

The module takes the form of a 4-layer printed circuit board (PCB). Various considerations must be taken into account when designing a PCB to ensure a high degree of signal integrity and low electro-magnetic interference (EMI). The steps taken to ensure this are highlighted in this chapter. Test-software is also developed to verify the functionality of the module, but will not be used in the eventual radar system.

After testing the hardware, it could be concluded that the module fulfils all the functional requirement set out in the beginning of the chapter and operates as intended. It must be noted that some minor alterations could improve the operation of the module, but are not essential for its functionality.

Chapter 5

In Chapter 5 the performance of the system will be evaluated. This phase measures the true success of the concept of IF cancellation and the hardware design.

First, spectral purity of the cancellation signal is measured. This measurement indicates that the DDS indeed generates a clean signal, with a narrowband Spurious-Free Dynamic Range (SFDR) in excess of 80dBC and wideband SFDR of 70dBC being measured. The phase noise of the generated signal is also measured here, and a plot of this measurement is included.

The second, and more important measure, relates to the level of cancellation that can be achieved. Two IF Cancellation Modules were used for this test - one generating an IF and the other generating a cancellation signal that is added to the IF. The test indicated that the possible cancellation exceeds 53dB and that the RMS error between the two signals is smaller than 4mV when the optimum phase difference and amplitude balance is achieved.

After the measurements are taken, the results are compared to those obtained from simulation. The comparison will show that the simulation model was accurate in its predictions pertaining to digital word lengths of amplitude and phase, but incorrect in predicting the RMS error between the IF and cancellation signals.

Chapter 6

The final chapter is an overview of this report and will draw conclusions from the results obtained during this dissertation. The most important of these conclusions is that the concept and physical incarnation of an IF Cancellation Module gives promising results. A high degree of cancellation is possible with the module and, with correct calibration, could dramatically improve the dynamic range of the SFCW GPR for which it has been designed.

1.3 Background to Problem

Before the problem addressed in this dissertation can be stated, the basic operation of SFCW radar must first be explained. The explanation given here merely serves to give a conceptual understanding of the architecture; for a full treatment of the topic, the reader is referred to Langman [40] and Noon [47].

As the name suggests, a SFCW radar transmits a number of frequencies, with equal steps between the different frequencies. An example of the frequency-time relationship of the transmit waveform is shown in Figure 1.1, where 'F_u' is the highest and 'F_l' is the lowest frequency transmitted.

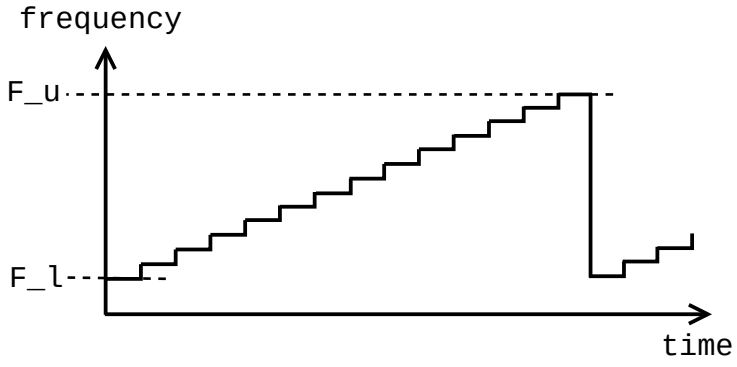

Figure 1.1: A frequency-time plot of the transmit waveform of a stepped frequency continuous wave radar

The reason for using some form of frequency modulation in the transmit waveform is two-fold. Firstly, CW radars work on the principle that the returned wave's phase shift is proportional to the distance to a target [40, 41]. If a single frequency were used, the unambiguous range of the radar would be limited to half the wavelength of that frequency [41]. In using more than one frequency, the range of the system can be increased. Secondly, the return from any one of the frequencies in SFCW is a single vector consisting of the sum of all the scattering vectors [36]. The contributing vectors can only be resolved by applying a Fast Fourier Transform (FFT) to a number of different frequencies.

The radar of interest in this dissertation uses a "Heterodyne Dual Synthesizer Architecture", as described by Langman [40]. A block diagram of such a system is shown in Figure 1.2.

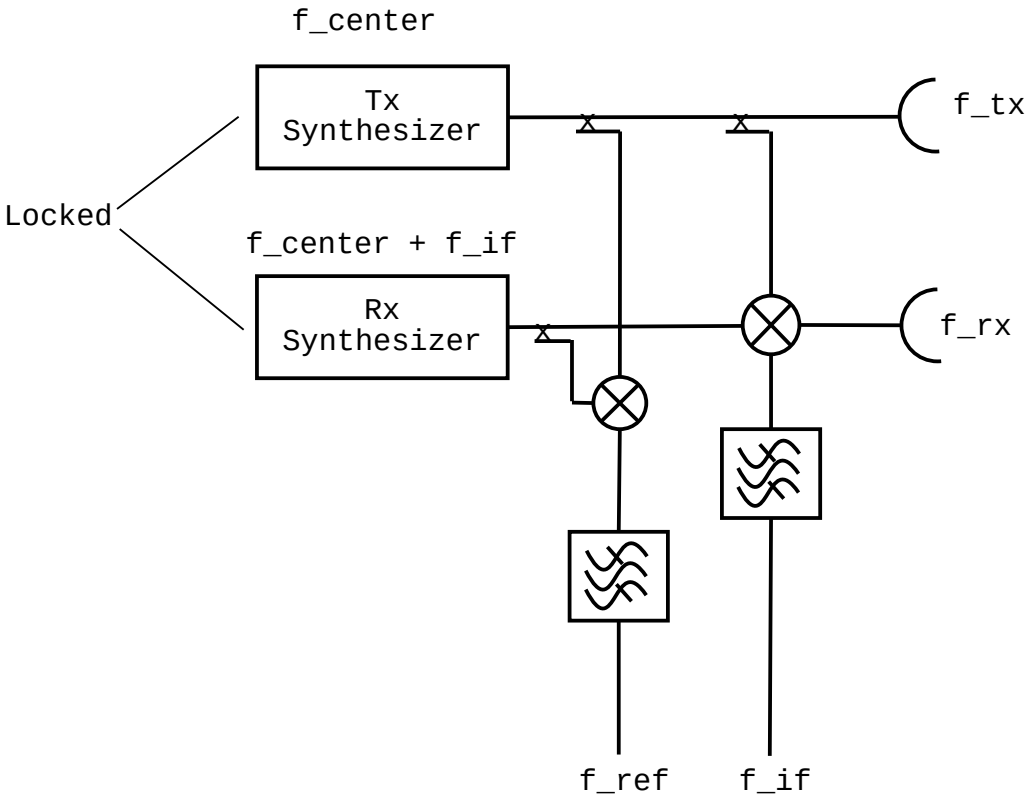

Figure 1.2: Block diagram of “Heterodyne Dual Synthesizer Architecture”, taken from Langman [40]

The system consists of separate transmit and receive synthesizers, locked to the same reference oscillator and offset in frequency by the system IF. The transmit waveform is amplified and radiated through the transmit antenna. Reflections from targets are received by a separate receive antenna and mixed with the receive synthesizer. The resulting signal is then filtered at the IF to remove harmonics, after which it is ready to be captured by an ADC for further processing.

Continuous Wave (CW) radars, as opposed to pulse radars, have both transmitter and receiver on at all times. One of the most severe difficulties encountered by designers of CW radar systems is the transmit-receive leakage problem, according to Stove [55]. This refers to electromagnetic energy that is coupled directly from the transmitter into the receiver. Skolnik [53] even suggests that CW radars can never be designed to meet a nominal power budget.

Kabutz, *et al.* [41] lists the effects of this leakage (in ascending order of severity) as

- Decrease in receiver sensitivity
- Saturation of the receiver
- Destruction of the receiver

The specific effect in any given situation is dependant on the transmit power levels involved, as well as the degree of isolation that can be achieved between transmitter and

receiver. Note that not all CW radars use separate transmit and receive antennas, but in the GPR in question in this dissertation, two antennas are used.

Kabutz, *et al.* [41] goes on to list various techniques to eliminate this feedthrough signal. The terms 'feedthrough', 'leakage' and 'direct coupled' signal will be used interchangeably in this document, but they all refer to the signal that is coupled directly between a transmitter and receiver in a CW radar system.

The applicable techniques described involve accurately characterizing and recreating the leakage signal with a 180^{o} phase difference. This recreated signal is then added to the original signal so that subtraction of the leakage is achieved. The cancellation circuitry can be placed either in the RF or in the IF stage of the system.

If placed in the RF stage, the cancellation system must be positioned immediately before the first IF mixer. This option must be taken if the RF receiver stage's dynamic range is not sufficient to accommodate the signal and feedthrough. The disadvantage of this approach is that the cancellation module would have to operate over the entire bandwidth of the SFCW radar.

If the RF stage can handle the signal and feedthrough, cancellation can be done in the IF stage. This is easier to implement, since cancellation only needs to take place at one frequency.

1.4 Problem Statement

The problem at hand can then be stated as follows:

> Design a hardware module that can generate a high quality (i.e. high SFDR) sinusoid at one particular frequency (the system IF) that is instantaneously adjustable in both amplitude and phase. The module must take as an input a signal of the same frequency and be able to add the generated signal to the incoming signal. The resulting signal after the summing process must be amplified to variable gain levels, depending on the requirements of the rest of the radar system.
>
> Show, through comprehensive testing that the designed module operates as intended and can be integrated into the SFCW-GPR for which it is designed.

To realize the solution, simulations will need to prove that the concept is viable. The rest of this paper describes the theory, simulation and design of a hardware module that meets these requirements.

Chapter 2

Theoretical Considerations of IF Cancellation

Chapter 2 presents the theory required to realize the IF Cancellation Module. Firstly, signal cancellation in the context of this paper is defined. It is shown that the most effective method of cancellation is adding two signals that are in exact anti-phase with respect to each other. Motivation for the use of Direct Digital Synthesis (DDS) will also be given.

The chapter then continues by explaining the operation of DDS. A breakdown of the system architecture will show that DDS has two main sources of error. Phase truncation and amplitude quantization produce spurious signals in the DDS output spectrum. The level of these spurs are dependent on the amplitude and phase resolution and a simulation will show that there is no significant gain in signal-to-noise ratio when one has more resolution in one than the other. This result is an important one and is used in the hardware design phase.

The next part in the chapter deals with phase noise in signal sources and oscillators. An ideal oscillator exhibits a perfect spike at its output frequency in the frequency domain. All real oscillators exhibit phase noise, however, and this causes a spectrum that is not infinitely narrow. Phase noise and its causes are discussed as a measure of frequency stability in the frequency domain. The time domain version of frequency stability, jitter, is also explained and it will be shown how to convert from a phase noise plot to a jitter figure. This conversion is essential, since it is used in the simulation of the IF Cancellation Module. Allan Variance, another measure of frequency stability is also documented for completeness.

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2.1 Definition of IF Cancellation

Consider a typical ground penetrating radar (GPR) scenario depicted in Figure 2.1.

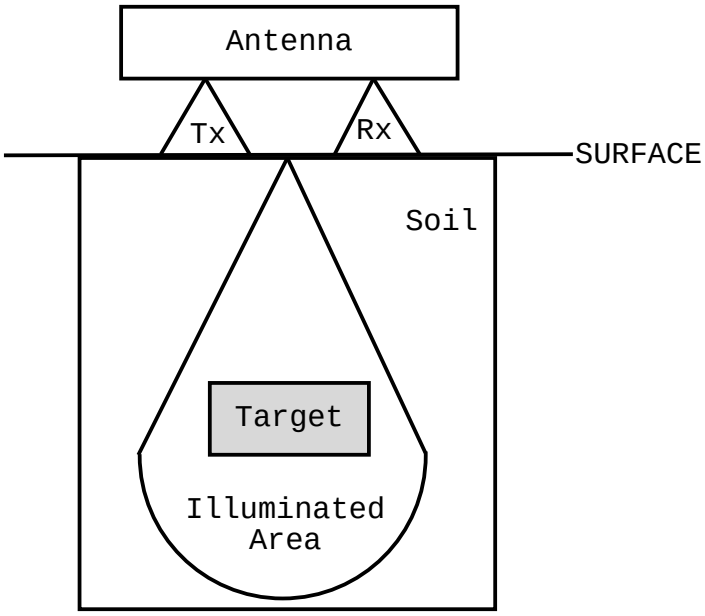


Figure 2.1: A typical GPR scenario

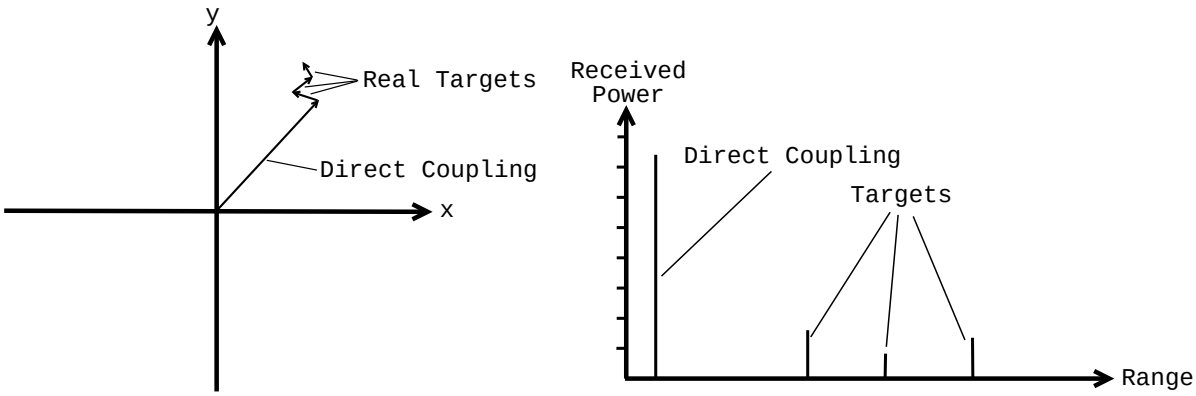
At some time, *t*, the transmit (Tx) antenna transmits a radar waveform $V_{tx}(t)$. The receive (Rx) antenna waits for reflected electromagnetic energy from a target or targets. Besides the energy reflected from targets, a large signal is coupled directly from the transmitter into the receiver. It must be noted that this phenomenon is encountered in all CW radars and is not confined to GPR [55].

This signal will be significantly larger than any signal reflected from a target. In terms of a radar range profile, it will appear as a large received signal at virtually zero range. The effect is that this large coupling signal effectively decreases the dynamic range of the system because it uses the full-scale input of the ADC. It can cause small target reflection not to be detected and can also mask smaller targets that are close to the radar during a single radar scan.

A vector representation and simplified radar range profile of this situation is shown in Figure 2.2. In the range profile, the Received Power (y) axis is scaled in the 8 quantization steps of a 3-bit ADC, which is used as an example to illustrate the problem.

As can be seen in Figure 2.2, the coupling signal is significantly larger than the target information. The received power in the range profile is scaled to accommodate the large feedthrough signal at the input to the ADC. This means that target 2 will not be large enough to toggle the ADCs least significant bit (LSB) and hence will not be detectable by the radar system.

It may be possible to detect target 2 if “stacking” is used. Stacking involves taking multiple measurements of the same area and averaging the results. Random components in



(a) (b)

Figure 2.2: (a) Vector diagram of typical received radar signal - reflections from targets plus direct feedthrough coupling, (b) Simplified radar range profile showing targets and direct coupling signal

the return signal such as background noise will average out statistically and real targets will become larger in amplitude and hence detectable by the system. Range profiles with different stacking numbers using the SFCW GPR simulation of Langman [40] is shown in Figure 2.3:

It is seen that a large number of stacks, more than 64, is required to make the targets visible. Even in this event, the target signals (at 3m and 6m range) are barely above the noise floor.

If the feedthrough signal could recreated and subtracted from the total signal and the result amplified, cancellation would be achieved and the situation would look as shown in Figure 2.4.

Now that the coupling signal has been removed, the target returns can be amplified and all three are detected by the ADC.

If stacking is used in this case, the following is seen by simulation:

As can be seen, after 64 stacks the targets are clearly visible above the noise floor. This compares favourably with the simulation results shown in Figure 2.3 in that fewer stacks are needed and the signal-to-noise ratio has improved. Since less stacks are required, more scans can be taken during a specific time.

Dynamic range in a system is defined as the ratio between the maximum allowable signal and the minimum detectable signal in that system. Since the minimum detectable signal has been decreased, this ratio will be bigger and an increase in the system dynamic range has thus been achieved.

2.1.1 Creating the Cancellation Signal

The most important aspect of this subtraction method of cancellation is accurately recreating the leakage signal. The leakage signal will be a series of sinusoids of varying am-

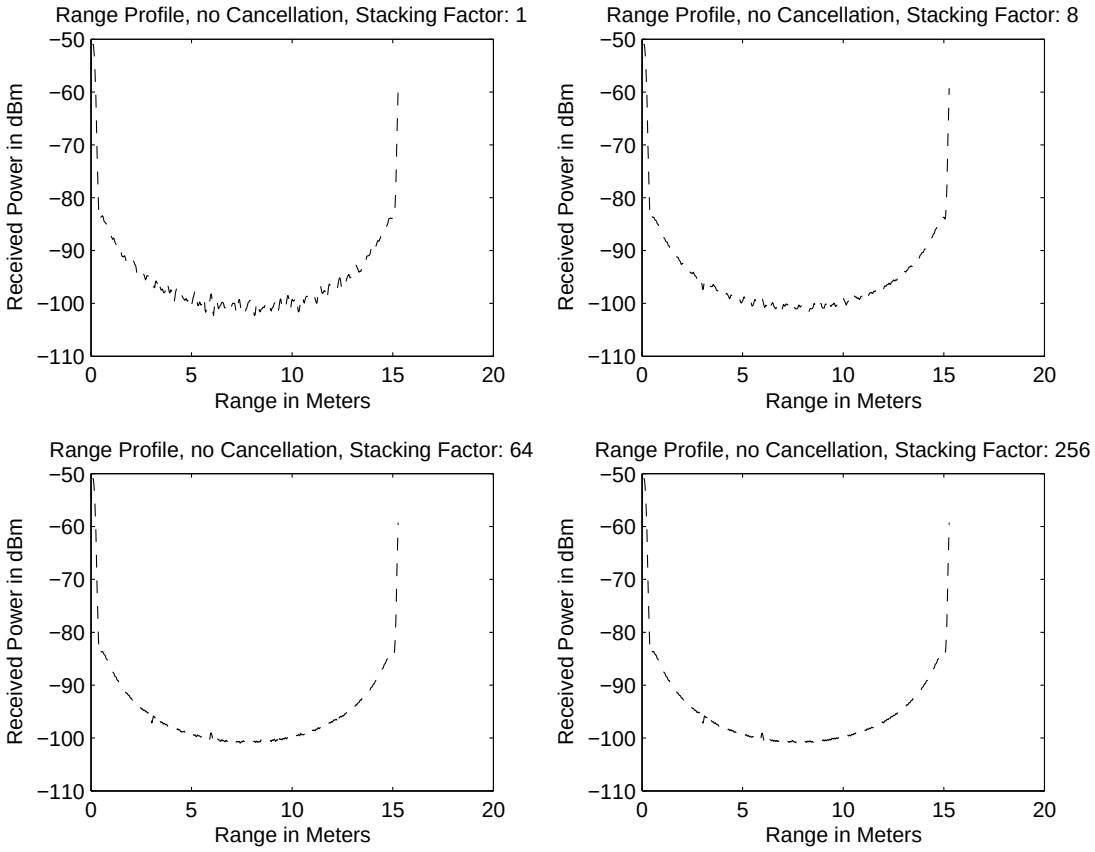
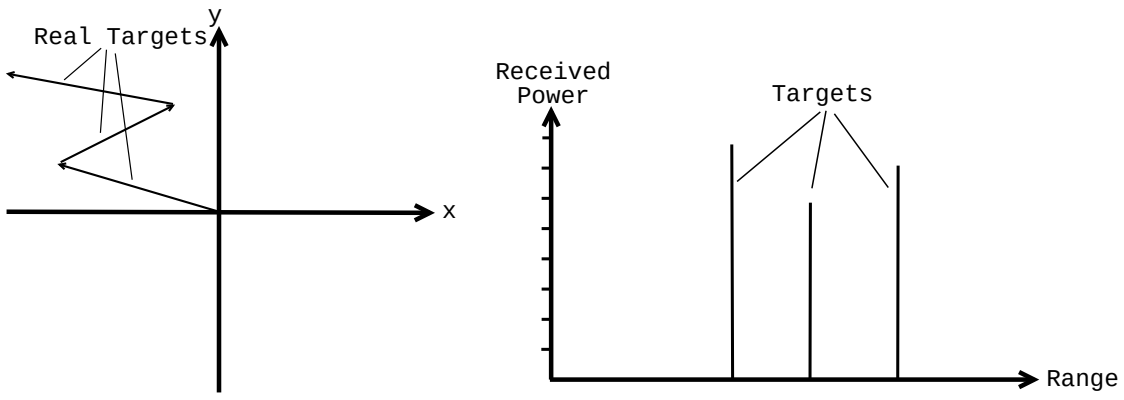


Figure 2.3: Four Range profiles with direct coupling signal and various stacking numbers



(a) (b)

Figure 2.4: (a) The returned radar signal with the feedthrough cancelled and the result amplified, (b) A range profile representation of (a)

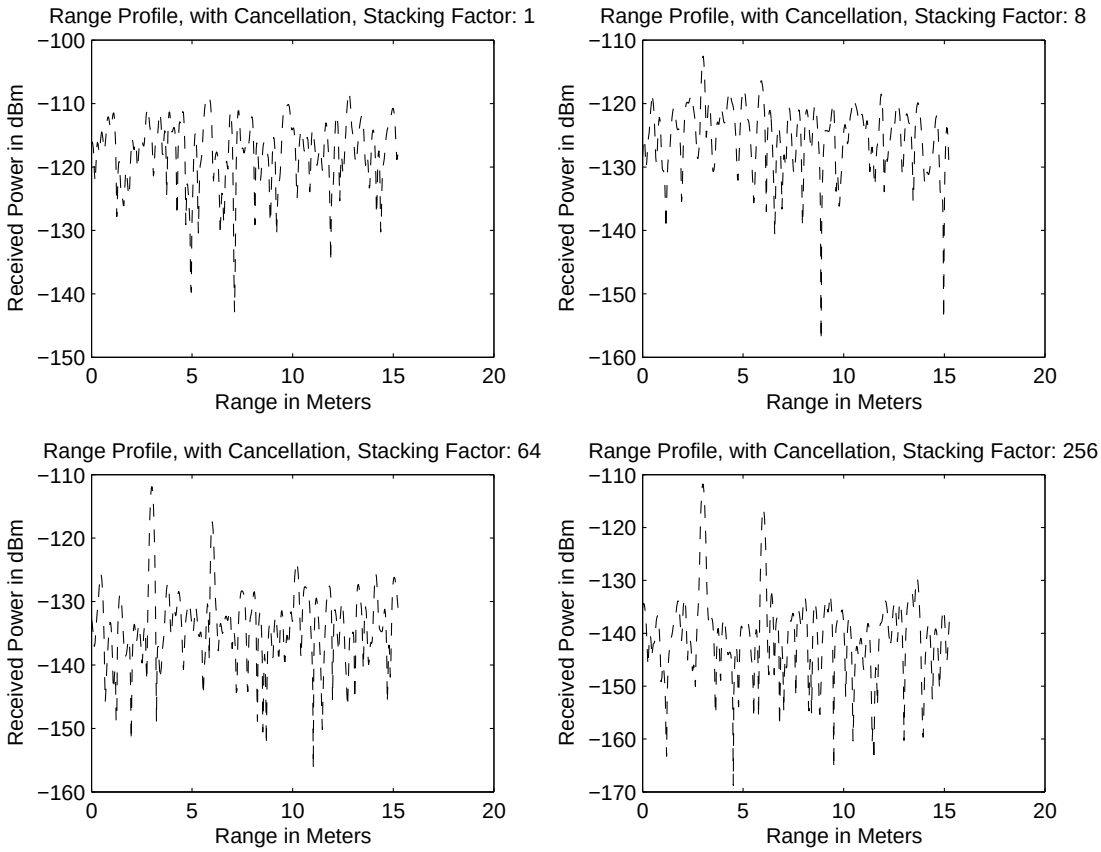


Figure 2.5: Four Range profiles after cancellation with different stacking numbers

plitude and phase at the system IF. This is due to the stepped-frequency transmit signal that is mixed down to the system IF not being phase continuous.

The phase difference between the received and cancellation signals is a very important consideration if the subtraction method is to be used. The only frequency synthesis method technique that offers phase control is DDS. Not only can DDS accurately set the phase of its output signal, but it can also switch to a different phase almost instantaneously.

From an electronic hardware design point of view it must also be noted that operational amplifier adder circuits are less complex and more accurate than their subtraction counterparts. It would thus be viable to create the cancellation signal in exact anti-phase to the leakage signal and then add it to the received signal.

2.1.2 Imperfections in the Cancellation Process

Perfect cancellation will not be possible, however. The least serious imperfection is an imbalance between the amplitudes of the feedthrough and cancellation signals. If these signals are in perfect anti-phase, the degree of cancellation will be proportional to the level of amplitude balance. This implies that the entire leakage signal will not be removed, but for small amplitude imbalances the cancellation will be near-perfect.

Phase imbalance has more drastic effects. Consider the situation where the amplitudes of the leakage and cancellation signals are equal, but their phase difference is not exactly 180^{o}. A vector diagram of this scenario is shown in Figure 2.6. For clarity, the contributions from other targets are ignored.

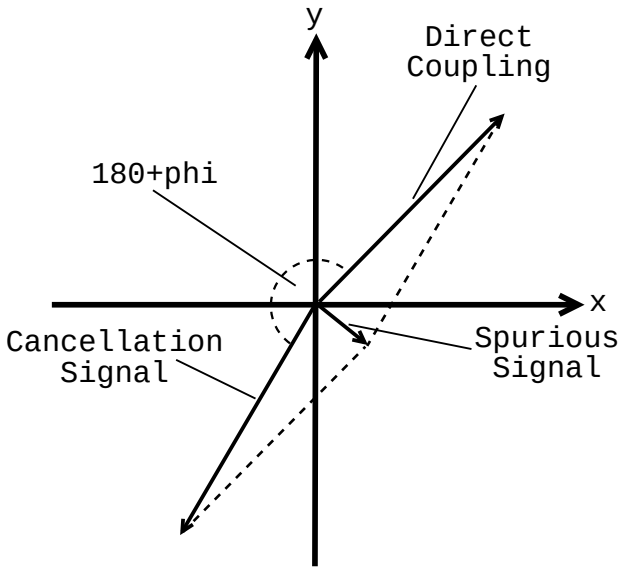


Figure 2.6: The creation of a spurious signal due to phase imbalance between the direct-coupling and cancellation signals

As can be seen in Figure 2.6, a spurious signal can be created if the feedthrough and cancellation signals are not exactly 180^{o} apart in phase. This is shown by simple vector addition. The magnitude of this spur is proportional to the phase imbalance. Three main factors will contribute to this phase discrepancy.

Firstly, the phase resolution of a Direct Digital Synthesizer, which is used to generate the cancellation signal, is limited. The phase is accurate to $\frac{360}{2^n}$ degrees, where *n* is the number of bits in the phase accumulator of the DDS. For *n = 12* (which is not uncommon in modern DDS), the phase resolution is 0.09^{o}. This may seem adequate, but it must be remembered that the signals reflected off real targets are of the order of -70dBm and even a small phase error such as this can cause a spur that is of the same order of magnitude as real targets.

Secondly, all signal sources exhibit phase noise. Ideally, a signal source produces a single spectral line with no energy at any other frequency. In reality this is never the case and phase noise is a measure of the energy in frequencies close to that of the source. It is usually denoted by $\mathcal{L}(f_m)$ and is defined as the noise power in a 1Hz bandwidth at an offset frequency f_m from the source's primary frequency [28].

These phase imperfections will be present in both the feedthrough and cancellation signals. Some of the phase noise will be correlated since all the signal sources in the system run from the same master reference: the system clock. The correlated phase noise should not present a problem, since it will be cancelled. There will also be uncorrelated phase

noise between the two signals as well as additive external noise, however, which is random in nature. The vector diagram below shows the implications of these random phase fluctuations.

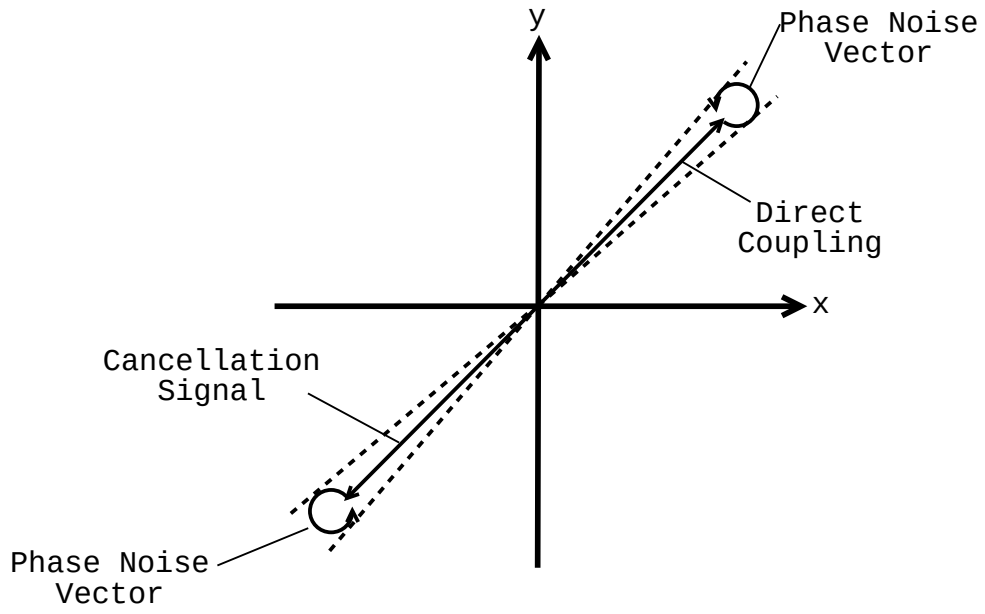


Figure 2.7: The feedthrough and cancellation signals in the presence of phase noise. The dotted lines represent the areas in which the phase of the signals could vary due to added phase noise vectors.

The dotted lines in Figure 2.7 represent possible positions of the two vectors. As can be seen, the presence of uncorrelated phase noise also results in spurious outputs, since it causes the directly-coupled and cancellation signals to not be in exact anti-phase. The phase error will not be a constant, however, and this will cause spurs to appear and disappear in a random fashion. This, in effect, will result in the system noise floor rising, which is undesirable.

The third cause of phase error is attributed to inaccurate calibration of the IF cancellation module. An algorithm will need to be devised that establishes a 180^{o} phase difference between the cancellation and feedthrough signals. This is what is meant by calibration in this paper. Failure of this algorithm to ensure the signals are in anti-phase will result in the same spurious signal being created as is shown in Figure 2.6.

2.2 Direct Digital Synthesis Explained

Direct Digital Synthesis (DDS) or a Numerically Controlled Oscillator (NCO) is the closest to an all-digital frequency synthesis technique available today. Goldberg [24] defines frequency synthesis as “a system that generates one or many frequencies derived from a single time base (frequency reference), in such a way that the ratio of the output to the reference frequency is a rational number.” A frequency synthesizer thus derives an output frequency (usually a sinusoid) from a clocking source by division or other means.

Thierney, *et al.* [57] proposed a Digital Frequency Synthesizer in 1971, but it has only been made feasible in the last 15 years by the massive evolution of digital electronics. Vankka, *et al.* [60] reports that in past years DDS has been limited to produce narrow bands of closely spaced frequencies. Recently, however, DDS systems with bandwidths of above 400MHz have become available from popular IC manufacturers.

A DDS system digitally builds a waveform from the ground up. This is in contrast to analogue synthesis techniques such as phase-locked loops (PLL) and Direct Analogue (DA) synthesizers which use oscillators as the main frequency generation mechanism.

2.2.1 Basic System Architecture

A block diagram of the DDS architecture is shown in Figure 2.8:

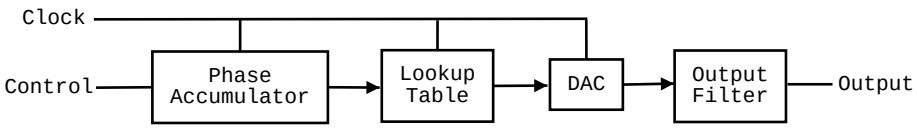


Figure 2.8: The basic Direct Digital Synthesizer system architecture. Note that the output filter is not strictly part of the system, but is included for completeness

The system clock acts as the frequency reference (from the definition of a frequency synthesizer above) in a DDS. The 'Phase Accumulator' is in effect a digital counter with variable increments who's output addresses a Lookup Table (LUT). The LUT usually takes the form of Read-Only Memory (ROM) containing uniformly spaced sampled values of a sinusoid for one cycle.

The LUT outputs the appropriate amplitude information as indexed by the Phase Accumulator. The output from the Phase Accumulator thus acts as the phase of the sinusoid, hence its name. The output from the LUT is fed to a Digital-to-Analogue Converter (DAC), which converts the data to the analogue-domain. From here the signal passes through a (usually external) low-pass filter to produce a smooth sinusoid.

The rapid phase changes required for the IF cancellation is easily achieved by simply initializing the accumulator with appropriate values.

2.2.2 Theory of Operation

The output frequency of a DDS is dependent on the 'frequency control word', *W*, which is a digital word presented to the input of the Phase Accumulator. For a *N*-bit accumulator and a reference clock frequency f_{clk}, the output frequency is given by

$$f_{out} = \frac{W.f_{clk}}{2^N},$$

where $W < 2^{\mathcal{N}-1}$. This constraint comes from the sampling theorem [60] and shows that the maximum theoretical output frequency of a DDS is limited to $\frac{f_{clk}}{2}$. In reality, the maximum useable output frequency is limited to about 40% of the clock reference [24, 60] due to the difficulty of filtering image frequencies close to the Nyquist rate. The accumulator has modulo $2^{\mathcal{N}}$ operation and overflows at the same rate as the output frequency.

The frequency resolution of a DDS system is

$$\triangle f = \frac{f_{clk}}{2^N}.$$

Given the levels of integration in modern-day digital electronics, it is easy to see that sub-hertz resolution is possible.

The output phase at any time index sample value *n* is given by

$$\theta(n) = \frac{2\pi n}{N},$$

and the output amplitude *A* for any *n* is then

$$A(n) = \sin(\theta(n)) = \sin(\frac{2\pi n}{N})$$

Note that this formula assumes no quantization effect of the sine-LUT and implies infinite word-length of the sinusoid samples in the LUT. In practice, the LUT will have limited precision and its output amplitude will be an approximation to the precise value of a sinusoid at that specific phase value. Quantization and its effect on a DDS system is considered in a later part of this chapter.

2.2.3 Spurious Signals in DDS

Apart from the wanted output signal, DDS also produces unwanted artifacts. These take the form of spurious signals (spurs) caused by the limited precision in the digital circuitry. Papay [48] claims that spectral purity is one of the most important specifications in synthesizers. He classifies the creation of spurs as "numerical distortion" and shows that amplitude quantization (AQ) and phase truncation (PT) are the main causes of degradation in spectral purity. Jenq [35] confirms this statement. INTEL [33] reports that spurious signals are the most significant limitation in DDS performance. The following sections will explain these sources of error and show their effect on the output spectrum of a DDS, but before AQ and PT are explained, note the following definitions of important DDS specifications, given in [6] for completeness:

1. Signal-to- (Noise + Distortion) Ratio

This is measured at the output of the DAC. The signal is the RMS magnitude of the fundamental frequency. The noise constitutes the RMS sum of power in all the other frequencies up to half the sampling frequency ($f_{\text{clk}}/2$), but excluding the DC component. It will be shown later that SNR = 1.76 + 6.02*m* dB, where *m* is the number of bits in the DAC output.

2. Spurious Free Dynamic Range (SFDR)

Harmonics of the fundamental, as well as images of the clock frequency will be present in the output spectrum of a DDS. SFDR refers to the difference in magnitude between the fundamental and the largest spur. There are sub-categories of wideband and narrowband SFDR. Garcia, *et al.* [21] explains further that SFDR must be measured over the Nyquist bandwith (wideband) and the band of interest (narrowband) in the system.

3. Total Harmonic Distortion (THD)

This is the ratio of the RMS sum of the harmonics to the RMS value of the fundamental. Expressed mathematically,

$$THD = 20\log\left(\frac{\sqrt{H_1^2 + H_2^2 + H_3^2 + ... + H_n^2}}{P_{fundamental}}\right),$$

where H_{n} is the highest order harmonic.

Amplitude Quantization

Due to the finite word-length of the sine-LUT, samples presented to the DAC will be approximations to the actual values of a sinusoid at a given phase [58]. This is what is meant by amplitude quantization.

For a sine-wave of amplitude *A* the signal power is $A^2/2$ watts [56]. The quantization error is evenly distributed over $[-\triangle_A/2, \triangle_A/2)$ and the error power is $\triangle_A^2/12$, where $\triangle_A = 2^{-m}$ and *m* is the number of bits in the amplitude word [56, 58]. For a long period of observation, the signal-to-quantization-noise ratio is then

$$SNR = 10\log\left(\frac{A^2}{2} \times \frac{12}{\triangle_A^2}\right)$$

$$= (1.76 + 6.02m)\, dB$$

This shows the ratio to improve by approximately 6dB for each additional bit in the digital word

The rounding operation implicit in quantization (minimum distance or nearest neighbour), as well as the fact that DDS output has odd symmetry causes odd harmonics of the fundamental frequency [48, 58] to be generated. The levels of the generated harmonics fluctuate wildly and it is complicated to calculate exactly, but Kester [37] reports that it is highly dependent on the ratio of output-to-clock frequency. If f_{out}/f_{clk} = *L/P* (some *L* relative prime to *P*) then the number of AQ-spurs is (*P/4) -1* [48]. Assuming that spectrum is calculated over the period, *P,* the carrier-to-spur power spectral density is given by Vankka [58]

$$\frac{C}{S} = 1.76 + 6.02m + 10\log(\frac{P}{4})\ dBc$$

Because of the sampling processes in DDS, some harmonics can also be aliased back into the band of interest. Papay [48] calculates that for *P* = 4 there is no quantization since the samples match the exact sinusoid values and only DAC nonlinearities cause DDS distortion. For *P = 8*, on the other hand, energy from all harmonics concentrate on one spur (by imaging/aliasing from other Nyquist zones) and causes a significant degradation in SFDR.

Phase Truncation

Although no spurs are generated due to phase truncation if f_{clk}/f_{out} is an integer (which will be the case in the IF cancellation module), the effect of PT in DDS will be shown for completeness.

Consider a DDS with a 32-bit phase accumulator. 2^{32} entries would be required in the LUT to convert each accumulator value to an amplitude. If 8-bit amplitude precision were used, the LUT would have to be 4-gigabytes in size. This clearly is not practical. The solution is to use a fraction of the most significant bits (MSBs) of the accumulator to address the LUT [22, 24]. The phase information is thus truncated.

In the literature, the part of the accumulator presented to the LUT is called the integer part and the discarded bits are known as the fractional part. If the frequency control word, *W*, contains a fractional part, the data points will be clocked out with a non-uniform phase increment. This creates the effect of presenting a non-uniformly sampled sine wave to the DAC [48]. Jenq [35] shows that a non-uniformly sampled sine wave contains spurious harmonic components. He calculates in a subsequent paper [34] that the maximum and minimum possible SNRs due to phase truncation are

$$S/N_{PT}(max) = 20\log(K) - 3.92\ dB$$

$$S/N_{PT}(min) = 20\log(K) - 5.17\ dB,$$

respectively, where *K* is the number of entries in the LUT. These formulae simply give an upper and lower bound on expected SNR due to phase truncation. Furthermore, if *W* is represented by an integer and fractional part, i.e. *W = R + Q/P* (*Q, P* relative prime to each other) then the number of harmonics, including the fundamental frequency, is given by *P* and their relative locations in the spectrum are dependant on *Q* [48]. Thus, if *P = 1,* then *W* is an integer and the only harmonic is the fundamental frequency and hence no phase truncation takes place.

Combined Effect of Amplitude Quantization and Phase Truncation on DDS Output Spectra

Vankka [59] gives expressions for the combined effect of both spur generating mechanisms in terms of *k*, the number of bits used to address the LUT and *m*, the number of bits in the amplitude word. The superposition principle is used in the analysis to obtain

$$SNR \approx 1.76 + 10\log\left(\frac{\pi^2/2}{2^{2k}} + \frac{1}{2^{2m}}\right)^{-1} \ [dB]$$

The noise power is divided into *P* spurs (*P* is also the number of samples in the spectrum) and the carrier-to-noise power spectral density is given by

$$\frac{C}{N} \approx 1.76 + 10\log\left(\frac{\pi^2/2}{2^{2k}} + \frac{1}{2^{2m}}\right)^{-1} + 10\log\left(\frac{P}{2}\right) \ [dBc],$$

where dBC denotes dB's below the carrier (fundamental) power level. A plot of the SNR versus *k* and *m* is shown in Figure 2.9.

As can be seen, the optimum points are when amplitude bits equal the phase accumulator bits. In other words, no significant SNR increase will be achieved by increasing either of the bit-lengths beyond the other. It will be seen in Chapter 5 that this result holds when measuring the system performance

Other Sources of Spurious Signals in DDS

It must be noted that there are other sources of error in a DDS. These include phase-noise in the reference clock, DAC nonlinearities and clock feedthrough. Phase noise and its effect on this system will be discussed in subsequent sections.

The effect of DAC integral and differential nonlinearities on spectral purity is complicated and beyond the scope of this writing. Goldberg [24], Intel [33] and Gentile [22] note, however, that these nonlinearities produce harmonics of the fundamental, but that their levels are impossible to predict exactly. This form of error is known as harmonic distortion.

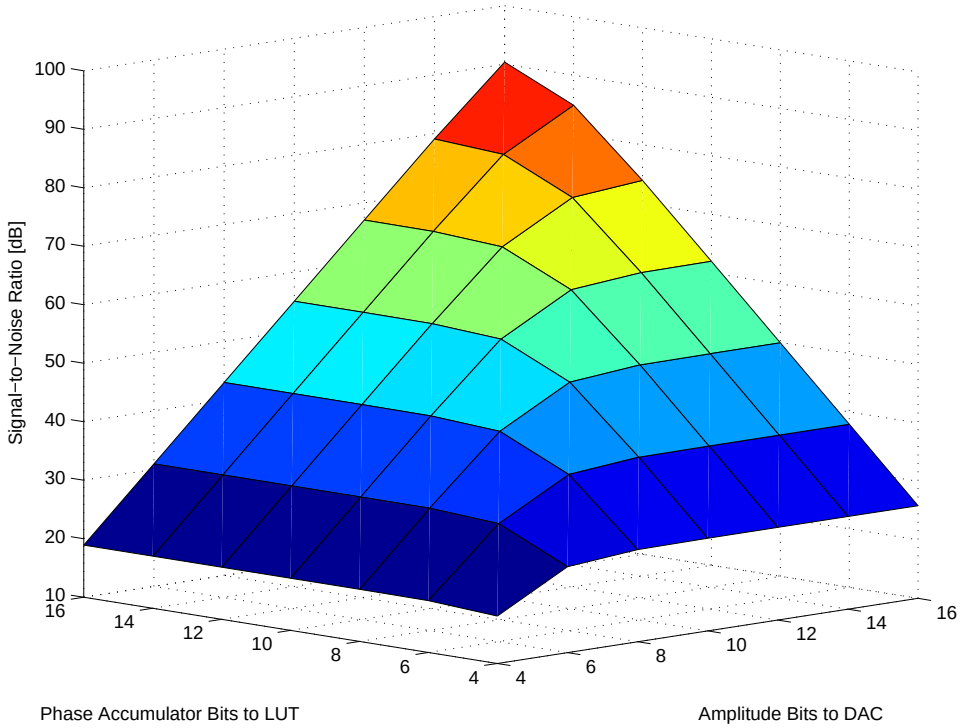


Figure 2.9: Plot of the Signal-to-Noise-Ratio of a DDS versus the number of amplitude and phase accumulator bits

Clock feedthrough refers to the fact that an attenuated version of the clock that drives the digital circuitry (and its harmonics) will be present in the spectrum of the analogue output signal [6].

2.3 Phase Noise, Jitter and Frequency Instability

This section will define and explain phase noise as a source of error in all frequency sources. It will be shown that phase noise (frequency domain) and jitter (time domain) essentially quantify the same phenomenon, namely frequency instability in oscillators.

The section contains descriptions of the most commonly accepted measures of frequency instability, including Allan Variance. The final part shows how the phase noise characteristic of an oscillator can be converted to jitter by means of a simple calculation.

2.3.1 Introduction to Phase Noise and Jitter

Consider the following representation of a perfect sine wave of amplitude *A* and angular frequency ω_o

$$v(t) = A\sin(\omega_o t)$$

Here, *v(t)* is the time domain version of a perfect sinusoid. The frequency domain version of *v(t)*, *V(*ω*)*, will consist of two δ (Dirac) pulses at $\pm\,\omega_o$ on the frequency axis. In reality,

however, the output from any sine wave generator or frequency source is actually given by [52, 31]

$$v(t) = [A + \epsilon(t)] \sin[\omega_o t + \varphi(t)],$$

where $\epsilon(t)$ and $\varphi(t)$ are random processes denoting amplitude and phase fluctuations, respectively. From standard amplitude and phase modulation theory [56], the presence of $\epsilon(t)$ and $\varphi(t)$ will cause modulation sidebands at frequencies offset from the carrier frequency (ω_o). This has the result of *V(ω)* not containing two δ's, but instead power-spectral densities of non-zero width [62].

A phasor representation of this modulation is shown in Figure 2.10.

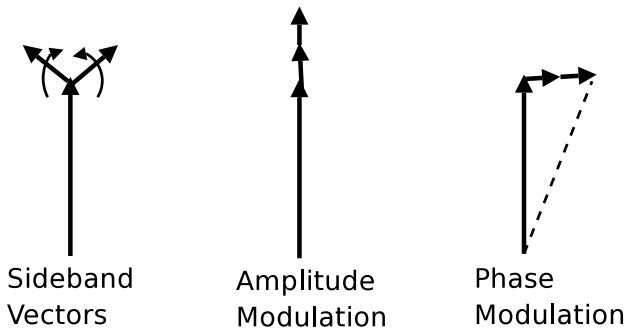


Figure 2.10: Phasor representation of modulation caused by sideband offset from the carrier frequency, taken from Robins [51]

In the above phasor diagram the rotating vectors represent the sidebands of the carrier. Depending on the alignment of the these vectors, they cause either pure amplitude modulation (AM), pure phase modulation (PM) or a combination of the two.

All treatments encountered pertaining to phase noise theory in oscillators assume negligible amplitude fluctuations $\epsilon(t)$. Some reasons for this is

1. High-quality oscillators have some type of amplitude stabilization [52],
2. RF mixers usually run at saturation power levels and are thus insensitive to oscillator amplitude fluctuations [25],
3. Limiter stages are often used in many systems as interface to a frequency reference and thus suppress amplitude variations [52].

For these reasons amplitude fluctuations can be ignored in phase noise analysis and the expression under consideration for a free-running oscillator is then simply [13, 5, 52]

$$v(t) = A \sin[\omega_o t + \varphi(t)]$$

Modulation of the carrier due to $\varphi(t)$ alone still causes phase modulation sidebands, characterized in the frequency domain by the spectral density $S_\varphi(f)$ and this is known as phase noise.

Jitter and phase noise essentially refer to the same phenomenon. Jitter, however, is a time domain representation of frequency instability, whereas phase noise is only defined in the frequency domain. In the discussion to follow, the main focus will be on the frequency domain measure of frequency instability although conversion to the time domain jitter parameters will also be shown.

Formal Definition of Phase Noise

Short-term frequency instability of a signal is usually described in terms of its single sideband noise spectral density. The units of this measure is "decibels below the carrier per hertz" (dBC/Hz) and the expression is defined as [26]

$$\mathcal{L}_{total}(\triangle\omega) = 10\log\left(\frac{P_{sideband}\left(\omega_0 + \triangle\omega,\, 1Hz\right)}{P_{carrier}}\right),$$

where $P_{sideband}\left(\omega_0 + \triangle\omega,\, 1Hz\right)$means the single sideband power at a frequency offset $\triangle\omega$ from the carrier in a 1Hz measurement bandwidth. It must be noted that this definition includes the effect of amplitude fluctuations $\epsilon(t)$, but, since this is regarded as negligible in most applications, $\mathcal{L}_{total}(\triangle\omega)$ can be seen as the pure phase noise of a signal and will henceforth be denoted $\mathcal{L}(\triangle\omega)$.

Grebenkemper [25] and Abidi [1] further show from phase modulation theory for small angles that

$$\mathcal{L}(\triangle\omega) = S_\varphi(f)/2$$

Allan, *et al.* [4] and Lance, *et al.* [39] confirm the above relationship and state that it only holds if $\int_f^\infty S_\varphi(f)df \ll 1radian$, i.e. the relationship is valid for *f* far enough from the carrier frequency. It will be seen later that spectral content close to the carrier is difficult to measure and impossible to predict exactly.

2.3.2 Leeson's Phase Noise Model

Leeson [43] in 1966 was the first to derive a simple, intuitive model for the noise spectrum of a feedback resonator oscillator [1]. In his model $\varphi(t)$ is treated as a zero-mean stationary random process that describes deviations from the ideal phase of the oscillator.

Leeson claims that a basic requirement for an oscillator noise model is that it must show clearly the relationship of the power spectral density $S_\varphi(\triangle\omega)$ of frequency to the known or expected noise and signal levels and resonator characteristics of the oscillator. Leeson's model gives a semi-empirical mathematical formulation for $\mathcal{L}(\triangle\omega)$ and his original work results in a typical power spectral density of phase as shown in Figure 2.11.

Zhang, *et al.* [62], Goldberg [23], Lee, *et al.* [42] and others have added correction factors to the original Leeson equation to account for *1/f* device noise (flicker noise, discussed

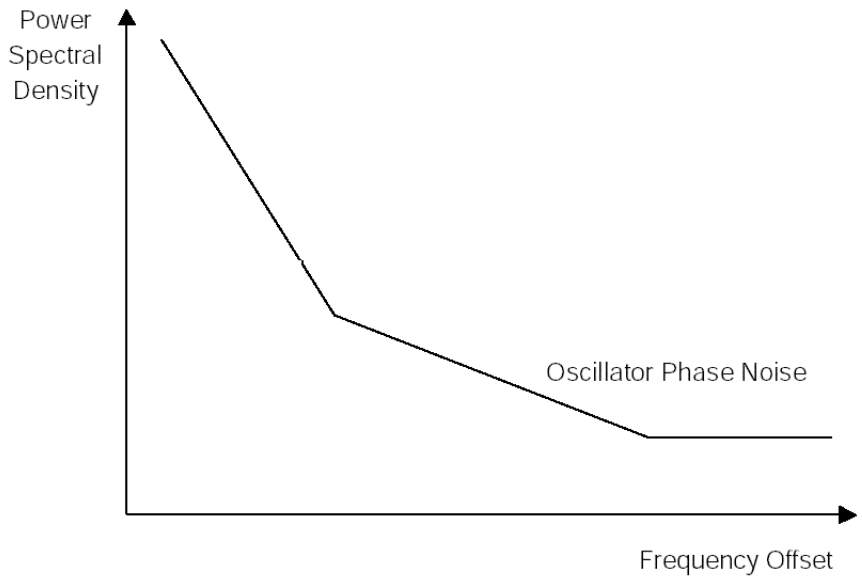


Figure 2.11: Typical power spectral density of phase as described by the Leeson phase noise model in 1966

shortly) in the oscillator. Currently, the most widely accepted formulation is

$$\mathcal{L}(\triangle\omega) = 10\log\left\{\frac{2FkT_{abs}}{P_{carrier}}\cdot\left[1+\left(\frac{\omega_0}{2Q\triangle\omega}\right)^2\right]\cdot\left(1+\frac{\triangle\omega_{1/f^3}}{|\triangle\omega|}\right)\right\},$$

where *k* is Boltzmann's constant, T_{abs} is a reference temperature, *Q* is the quality factor of the resonating device, $P_{carrier}$ is the average power of the carrier. *F*, the "device excess number" and $\triangle\omega_{1/f^3}$ are fitting parameters that must be measured empirically. $\triangle\omega_{1/f^3}$ is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions as shown in Figure 2.11. Also in Figure 2.11, the Leeson model shows a $\frac{1}{f^\alpha}$ power law dependency, where *f* is the frequency offset from the carrier and α is an integer from 0 to 3. Goldberg [23] interprets the data as follows:

1. At frequencies close to the carrier, the noise declines at 30dB/decade frequency offset ($\alpha = 3$)
2. At the frequency given by $\triangle\omega_{1/f^3}$, the noise declines by 20dB/decade, i.e. $\alpha = 2$
3. The noise continues to decline at 20dB/decade until it reaches a noise floor, where $\alpha = 0$

In the following section the origins of this power law dependency will be shown and it will be seen that the noise spectrum is actually a composition of five noise processes.

2.3.3 Power Law Noise Processes in Oscillators

Frequency sources contain noise that appear to be a superposition of causally generated signals and random, non-deterministic noises [39]. Many papers contained in the National Institute of Standards and Technology (NIST) Technical Note 1337 explain the typical phase noise behaviour of an oscillator as being the result of a combination of five noise processes. These noise processes are models of precision oscillator noise that produce a particular slope on a spectral density plot [31]. The noise originates at baseband and gets up-converted to sidebands close to the carrier frequency by means of the nonlinearities inherent to an oscillator.

Each process has an integer value for α and has been given a name. This section will define these noise sources and attempt to explain the origin of each.

a) Random Walk FM (Random Walk of Frequency)

This noise occurs close to the carrier frequency and drops off as $1/f^4$. It is difficult to measure. Lance, *et al.* [39] relates the noise to the oscillator's physical environment and offers factors such as mechanical shock, vibration and temperature as possible causes. Lesage, *et al.* [44], however, claims that the true origins of this noise is still not well understood. Since its origin is not well known, it is impossible to predict and is usually not included in the phase noise specification of a frequency source. Random walk FM is a source of long term frequency instability.

b) Flicker FM (Flicker of Frequency)

Flicker frequency modulation subsides with a $1/f^3$ power law on a plot of $\mathcal{L}(\triangle\omega)$. Its presence can be attributed to the direct up-conversion of baseband $1/f$ (or Flicker) noise which is usually present from 1Hz to about 10kHz. Howe, *et al.* [31], Hooge [29] and Robins [51] claim that the origin of $1/f$ noise is still largely unknown. Lance, *et al.* [39] relates the noise to the physical resonance mechanism in the active oscillator, as well as active electronic components in the device and environmental properties.

$1/f$ noise sources and its analysis is a large topic of discussion. For a full review of the subject, the reader is referred to Hooge [29].

c) White FM (White Frequency, Random Walk of Phase)

This noise is commonly found in passive-resonator frequency standards [31, 39] and goes down on a $\mathcal{L}(\triangle\omega)$ plot as $1/f^2$. Drucker [19] describes white FM as broadband noise that is shaped by the *Q* (quality factor) of the oscillator. It arises from additive white noise sources internal to the oscillator loop [52] such as thermal noise .

d) Flicker PM (Flicker Modulation of Phase)

Flicker PM noise is usually introduced by noisy electronics and frequency multipliers, although it could also be related to the physical resonance mechanism in the oscillator [31]. This from of noise is found in the highest quality oscillators [39]. The level of Flicker PM decreases with $1/f$ and can be reduced by careful component selection and negative feedback [52].

e) White PM (White Phase)

White PM noise has little to do with the resonance mechanism in an oscillator and is classified by Howe, *et al*. [31] as broadband phase noise. It has a flat (f^0) spectrum and appears as a noise floor on a plot of $\mathcal{L}(\triangle\omega)$. Lance, *et al.* [39] and Howe, *et al. [31]* conclude that white PM is caused by the same sources as Flicker PM and that careful component selection can successfully reduce the level of this broadband phase noise.

Combining the Noise Processes

Shown in Figure 2.12 is a graphical depiction of the power law noise processes discussed above.

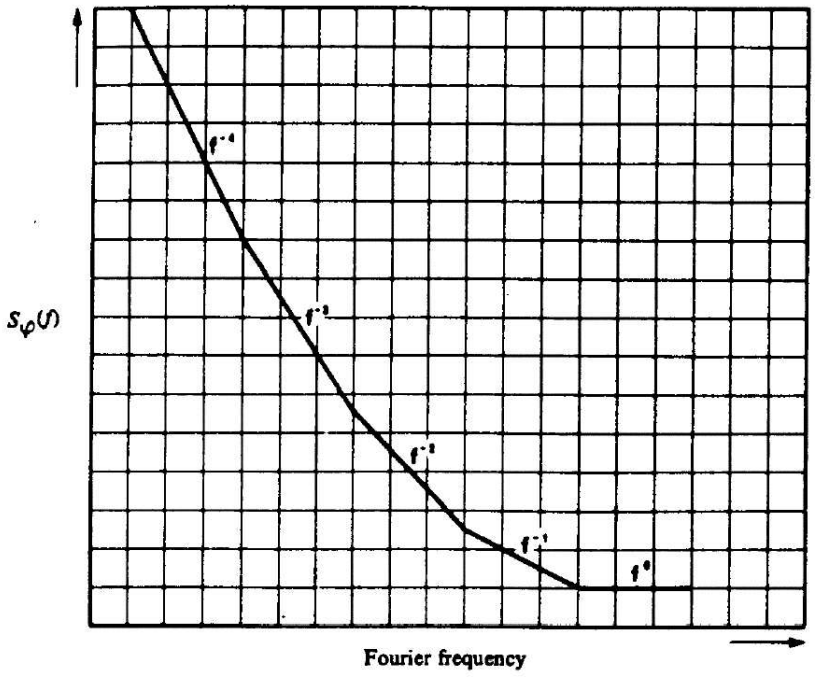


Figure 2.12: A plot of the 5 noise processes as described above

Most oscillators typically have two or three different power law slopes on a plot of $\mathcal{L}(\triangle\omega)$ and would not have phase noise characteristics as shown in Figure 2.12 [31]. A more realistic phase noise plot is seen in Figure 2.11 , where there are only three distinct slopes and the phase noise is a combination of the five noise sources.

2.3.4 Jitter and Allan Variance

Jitter is a statistical measure of a noisy oscillation process, i.e. each oscillation period is different due to noise-induced jitter [50]. It is the time domain representation of phase noise, which is only defined in the frequency domain. Drakhlis [18] defines jitter as the short-term non-cumulative variations of significant instants of a signal from their ideal positions in time. The variations can be ahead or behind the ideal positions. Significant instants generally refer to the zero-crossings of an oscillator output [32]. "Short-term" is commonly accepted as implying variations in frequency at a rate greater than or equal to 10Hz [14].

The two most commonly used jitter specifications are briefly discussed below, after which Allan Variance will be defined. It must be noted that there is great ambiguity in the literature about the definitions of the various jitter measures. Consequently the definitions are taken from several publications that show the most correlation.

Period Jitter

Period jitter, also called short-term jitter, compares the duration of each cycle period with that of an ideal/nominal period [13, 15]. The objective is to establish the variance in the period of a single cycle. It is the most common interpretation of jitter and it is expressed mathematically as

$$\sigma_p^2 = \lim_{N\to\infty}\left(\frac{1}{N}\sum_{n=1}^{N}(\tau_n - \tau_{ave})^2\right),$$

where τ_{ave} is the nominal cycle period and *N* is the number of samples taken.

Cycle-to-Cycle Jitter

This form of jitter is the most difficult to measure [15]. Cycle-to-cycle jitter is a measure of the variance of the difference in period of two adjacent sample cycles. Mathematically it is defined as [50, 51]

$$\sigma_{cc}^2 = \lim_{N\to\infty}\left(\frac{1}{N}\sum_{n=1}^{N}(\tau_{n+1} - \tau_n)^2\right),$$

where *N* is the number of samples taken and τ_n is the period of the n-th cycle. Poore [50] further shows that $\sigma_{cc}^2 = 2\sigma_p^2$.

Allan Variance

The 'Allan Variance' was accepted by the IEEE as the recommended measure of frequency stability in the time domain in 1971 [9]. It is also widely referred to as the 'two-sample variance'. Although it will not be used explicitly in any simulations to follow, its

discussion is required to ensure a complete account of frequency stability. The following explanation of Allan variance is taken from Howe, *et al.* [31].

It must first be understood that frequency measurements always involve two oscillators, where one of them is usually inside the measurement equipment. The fractional frequency deviation or difference of oscillator v_1 with respect to a reference oscillator v_0 is then defined as

$$y(t) = \frac{v_1 - v_0}{v_0},$$

where $y(t)$ is a dimensionless quality. The time-deviation of an oscillator over a time *t* is then given by

$$x(t) = \int_0^t y(t')dt'$$

It is impossible to measure instantaneous frequency, since this would require an infinitely short sampling time from the measurement equipment. There is always some time-window τ over which the oscillator is observed. The average fractional frequency over time τ is then defined as

$$\bar{y}(t) = \frac{x(t+\tau) - x(t)}{\tau},$$

where τ is often called the sampling or averaging time and is determined by the gate time of the measurement equipment (usually a frequency counter).

A logical way to extract the statistical properties of $\bar{y}(t)$ would be to calculate its variance and standard deviation. Howe, *et al.* [31], Stein [54] and others show, however, that these statistical properties increase as the number of measured data points increase when non-white noise sources are present in the oscillator. In Section 2.3.3 it was seen that flicker noise also modulates the oscillation frequency and hence traditional statistical measures are of no value, as it depends on the number of sample points. For this reason the Allan variance was proposed and is mathematically expressed as [52]

$$\sigma_y^2(\tau) = \frac{1}{2(M-1)} \sum_{k=1}^{M-1} (\bar{y}_{k+1} - \bar{y}_k)^2,$$

where *M* is the number of sample points and τ is the gate time of the measurement equipment. Note that the Allan variance assumes zero dead-time. Dead-time is caused by time-delays due to processing in the measurement equipment that, in turn, causes information of the oscillator signal to be lost.

2.3.5 Conversion Between Frequency and Time Domain Measures of Frequency Stability

It will be seen later in this report that it is easier to incorporate frequency instability in a system simulation by using time domain measures (jitter, Allan variance) rather than the phase noise specification $\mathcal{L}(\triangle\omega)$ in the frequency domain. For this reason it is necessary

to be able to convert from the phase noise spectrum of an oscillator to the desired time-domain equivalent of instability.

Converting from the time domain to $\mathcal{L}(\triangle\omega)$ is not a trivial task and many papers claim that it cannot be done. McFerran [46] says that time-domain data does not contain enough information to reconstruct the power spectral density of an oscillator exactly, although it can be approximated by a conversion table using the power-law model discussed previously. There are , however, papers that show attempts to do this conversion, most notably Hajimiri, *et al.* [27], Demir, *et al. [17]* and Zanchi, *et al.* [61], but it is beyond the scope of this paper.

Converting from phase noise to jitter basically involves integration of the phase noise plot $\mathcal{L}(\triangle\omega)$. The bandwidth of integration is an important factor in the phase noise conversion, since it directly influences the calculated jitter-number. The system in which the phase noise specification is being used must therefor be examined to establish an upper frequency limit for the integration.

Phase Noise to Jitter Conversion

As mentioned, jitter is calculated from a phase noise plot by integration. Various papers describe this process, with slight differences between them. This explanation is taken from Adler [2] and Fordahl [20]. The method was verified by comparing the result calculated from a phase noise specification of an oscillator with the jitter spec. An example calculation is shown in Appendix A

The first step is to identify the power-law slopes ($\frac{1}{f^a}$) and their respective positions in the plot of $\mathcal{L}(\triangle\omega)$. The phase noise value (in dBC) at the lower offset frequency corner of each of these slopes is then converted to noise power in watts. This value is multiplied by the area under that particular part of the curve, calculated by integration. That is

$$P = p_{watts} \times \int_{f_{low}}^{f_{hi}} \mathcal{L}(f)df$$

The contribution from each part of the curve is then summed to produce the equivalent sideband power at the maximum frequency of integration. Mathematically, this is expressed as

$$P_{total} = P_1 + P_2 + P_3 + ... + P_n$$

where $P_n$is the last unique slope in the phase noise plot.

Next $P_{total}$is converted back to dBm and the quantity, P_{dBm} is known as equivalent sideband level of the integrated phase noise. The calculated sideband is treated as small-index phase modulation, which allows one to calculate the phase deviation. Jitter can be expressed in various units. RMS Jitter in degrees is given by

$$J_{degrees} = \frac{360}{2\pi} \times 10^{\frac{P_{dBm}}{20}}$$

Similarly, the RMS jitter can be calculated in seconds. For an oscillator of frequency f this is given by

$$J_{seconds} = \frac{J_{degrees}}{f \times 360}$$

An example of this calculation can be found in Appendix A where the phase noise curve of a real oscillator is used to show that the calculated jitter value matches that of the oscillator specification.

2.4 Effect of Phase Noise and Amplitude and Phase Errors on Radar System

This section will demonstrate the success of perfect cancellation, as well as the effects of the various imperfections discussed thus far in this chapter, by means of simulation. The simulation was originally developed by Langman [40] for use in his thesis. Modifications were made to the software to accommodate phase noise and amplitude and phase errors.

The output of the simulation is in the form of radar range profiles and it will be seen that the signal quality deteriorates as each of these errors are introduced. The simulation merely serves to show that the imperfections do indeed affect the signal quality negatively and should not be seen as a quantitative attempt. The errors, however, are realistic in magnitude and can be reasonably expected in the radar system.

The final part of the simulation will show that when all these errors are present, the range profile deteriorates to the point where it is difficult to distinguish between detected targets and noise.

2.4.1 Perfect Cancellation

For the purpose of this simulation the leakage signal (to be cancelled) is modelled as a “large target” at close range. The first two profiles show that a small target that is close to the radar can be masked by this feedthrough signal (Figure 2.13). After perfect cancellation and amplification, the small target at close range is visible (Figure 2.14).

The range profile of Figure 2.13 indicates that there is only one detected target at 6 meters. The large return at virtually zero-range is the leakage signal. After perfect cancellation, however, it is seen that there are in fact two targets, one of them being masked by the leakage signal prior to cancellation.

The profile of Figure 2.14 clearly shows the presence of a second target at a range of 0.5m. It has been established that perfect cancellation will be impossible, though, so the following sections show the effects of imperfect cancellation.

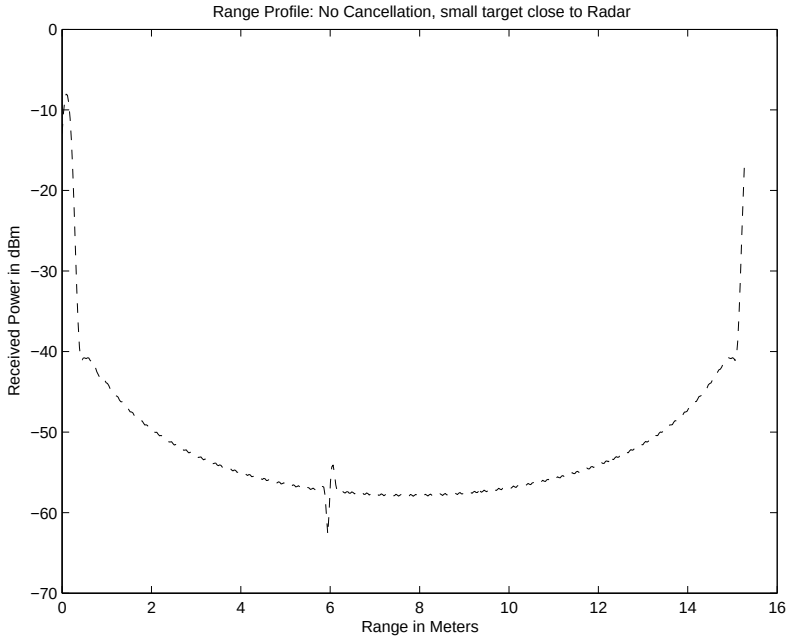


Figure 2.13: Feedthrough signal creates the appearance of only a single target

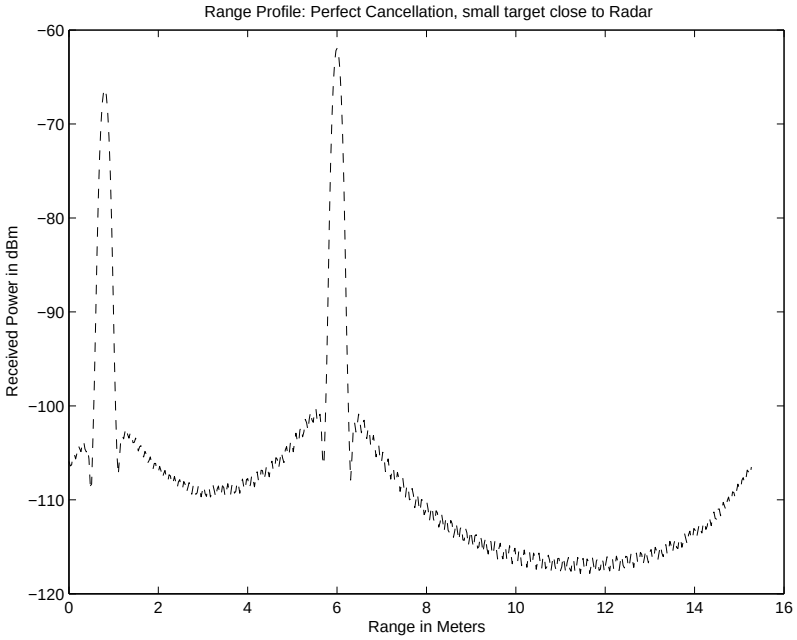


Figure 2.14: After cancellation and amplification, two targets are visible

2.4.2 Effect of Phase and Amplitude Errors in the Cancellation Signal

Figures 2.15 and 2.16 show the effects of amplitude and phase differences between the leakage signal and the generated cancellation signal, respectively. There are two targets in the simulation. The amplitude offsets can be attributed to quantization errors in the DDS, as well as incorrect calibration of the cancellation system.

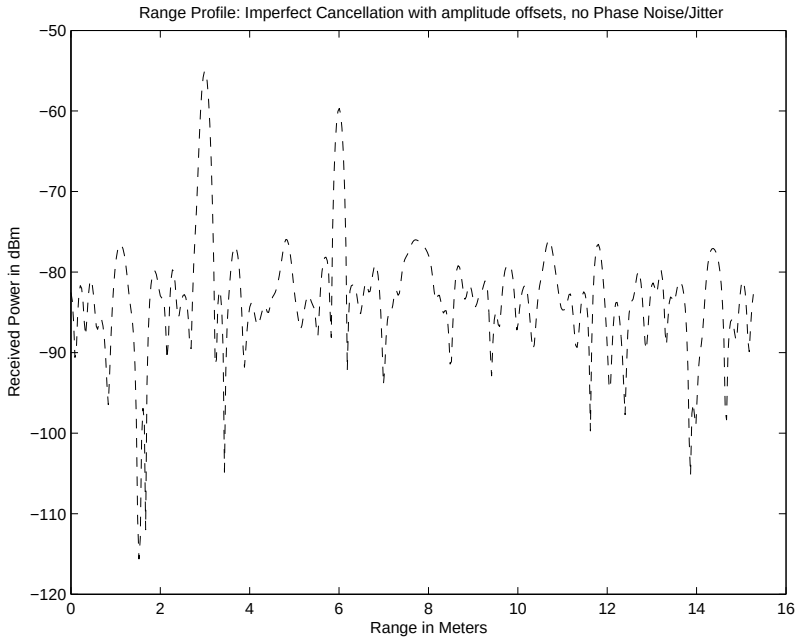


Figure 2.15: Range profile showing the deterioration in Signal-to-Noise ratio due to amplitude error

As can be seen in Figure 2.15, the noise floor of the range profile has increased and, although still visible, the targets are smaller in relative amplitude compared to Figure 2.14. Next, amplitude error is made zero and small random phase offsets between the leakage signal and the cancellation signal are introduced.

Once again, it is seen in Figure 2.16 that phase errors heighten the noise floor and thus decrease the SNR. These offsets will occur if the cancellation module is not properly calibrated.

2.4.3 Effect of Phase Noise in Transmit, Receive and Cancellation Synthesizers

As mentioned before, phase noise is present in all frequency sources. In the following simulation phase noise is first introduced in the transmit and receive synthesizers, and then also in the cancellation signal. Note that the phase noise plot of the actual oscillator in the system was integrated using the method above to obtain a jitter estimation. The calculation showed that a period jitter of 0.059^{o}RMS can be expected in the transmit,

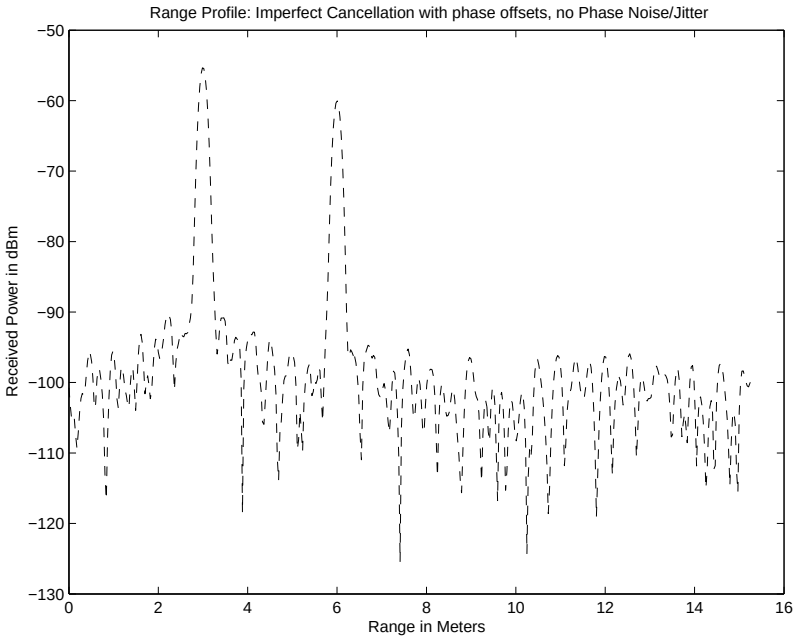


Figure 2.16: Range profile showing the effect of random phase errors between the leakage and cancellation signals on the radar signal quality

receive and cancellation signals. This jitter number was then used in the simulation to ensure realistic performance. An example of this calculation can be found in Appendix A.

Shown in Figure 2.17 is the effect of adding jitter to the transmit and receive synthesizers.

As with phase and amplitude errors, phase noise lowers the signal quality by adding noise into the system. Adding phase noise to the cancellation signal as well, produces a range profile as shown in Figure 2.18.

The range profile shows quite a dramatic increase in the noise level. Although the targets are still higher in amplitude, spikes that could be mistakenly interpreted as smaller targets are beginning to surface.

2.4.4 Combined Effect of All Sources of Error on the Radar Signal

In this final simulation, all the aforementioned sources of error are combined to show the total effect. Consider the range profile shown in Figure 2.19.

Phase offset was set to 0.4^{o}, 14-bit amplitude quantization was used and period jitter was given as 0.059^{o}RMS. The range profile has now deteriorated to a point where there are noisy spikes that exceed the amplitude of the smaller second target. If multiple radar scans are done, the data could be integrated and the quality will improve. The simulation does, however, show that careful design and accurate calibration will be required in order to minimize the errors and hence to successfully cancel the leakage signal.

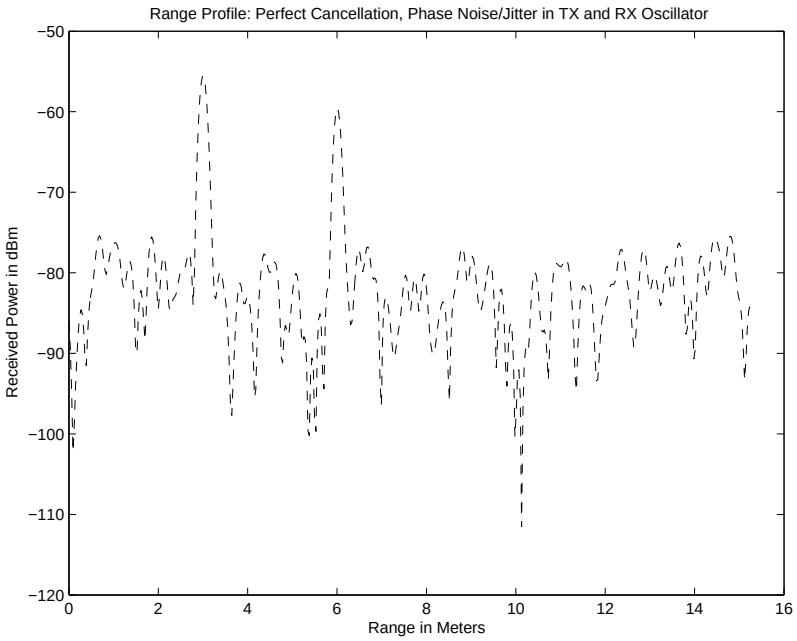


Figure 2.17: The effect of phase noise in the transmit and receive synthesizers on the radar signal. Cancellation signal is assumed to be perfect

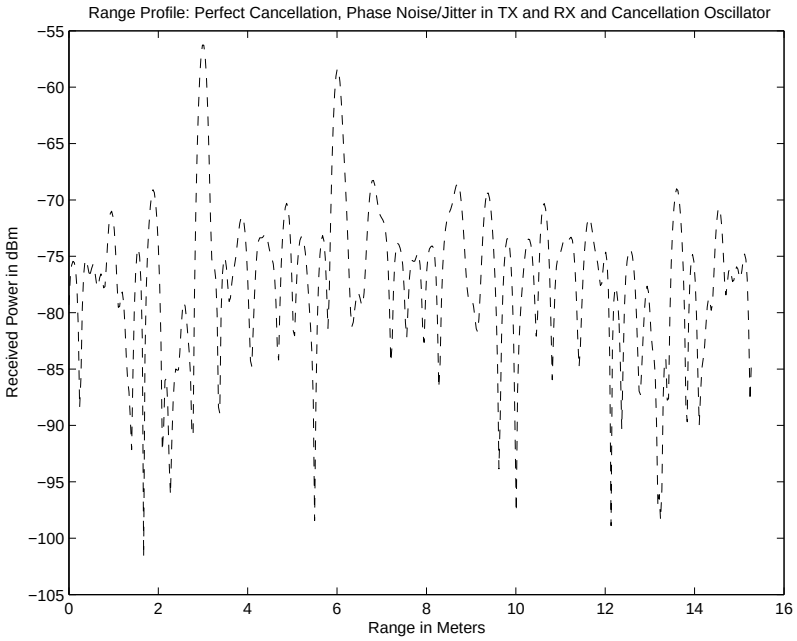


Figure 2.18: The radar range profile when phase noise is added to the transmit, receive and cancellation synthesizers

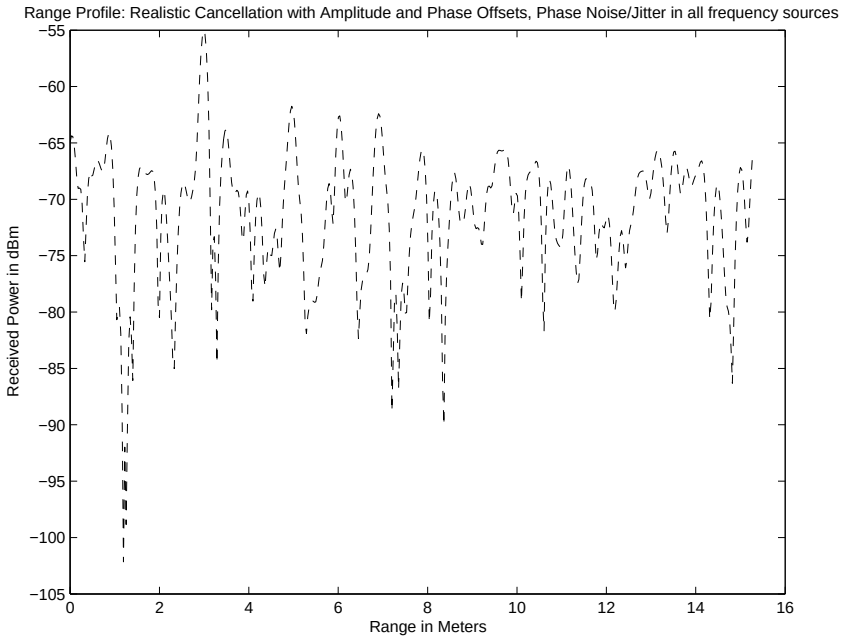


Figure 2.19: Range profile showing the combined effect of all the sources of error

2.5 Review of Chapter 2

In this chapter IF Cancellation was defined in the context of this dissertation. It was seen that the directly coupled signal can be subtracted/cancelled by recreating the signal with a 180^{o} phase difference and adding it to the total received radar signal.

Simulations in Section 2.1 showed that by cancelling the leakage signal, fewer stacks (shorter integration period) would be needed to detect a true target. The dynamic range of the system would be increased, since the entire input range of the ADC (which captures the data) can be used productively. Phase noise, as well as phase and amplitude errors were identified as the main sources of error in the cancellation process.

Direct Digital Synthesis (DDS) was identified as the synthesis technique that would generate the cancellation signal, since it offers fine control of phase. The DDS architecture was explained and it was shown that amplitude quantization and phase truncation are sources of spurious signal generation in the DDS output spectrum. A simulation indicated that no gain in signal-to-noise ratio is achieved by having more amplitude than phase bits and *vice versa.*

Frequency instability as a source of error was discussed next. Phase noise and jitter are the most common ways of quantifying small variations in frequency in the frequency and time-domain, respectively. A method for converting between the two measures was shown.

In the final part of the chapter the effects of the various imperfections in the cancellation process were shown by simulation. It was found that phase and amplitude errors as well as phase noise in the various synthesizers in the system caused deterioration in the returned signal quality and hence in the radar range profile. The simulation was not intended to be

quantitative, but rather to show the effect of these imperfections.

Chapter 3

Simulation of the IF Cancellation Module

In Chapter 3, a model for the IF Cancellation Module is developed. The objective of the model is to create a simulation of the system which will show the effects of phase noise and quantization in the DDS and IF signals on the cancellation process.

The model includes the RF stage of the radar system. The transmitted signal is mixed with a receive signal and bandpass filtered to produce the system IF. The transmit and receive signals both contain phase noise, but the noise is largely correlated.

The cancellation signal is then generated, using exactly the same architecture as a real DDS would. The quantized DDS signal is filtered and added to the IF. The simulation shows the effects of phase noise in both the IF and the cancellation signal at various bit resolutions for the DDS. An important result is that there is no improvement in cancellation at relatively high levels of phase noise if the DDS output resolution is increased beyond 10 bits.

The main shortcoming in the simulation is the modelling of the IF bandpass filter. This could not be modelled accurately, since the MatLab filters are difficult to edit. After some experimentation, the results seem promising, however.

3.1 Simulation Model

The MatLab simulation of the system is based on the block diagram shown in Figure 3.1. The code used to realize this model is included on the attached compact disc named Appendix B in the file 'if_canc.m'.

TX and RX denote the transmit and receive signals, respectively. A function was written that takes the following input parameters:

1. Number of cycles for simulation
2. Number of samples per TX cycle

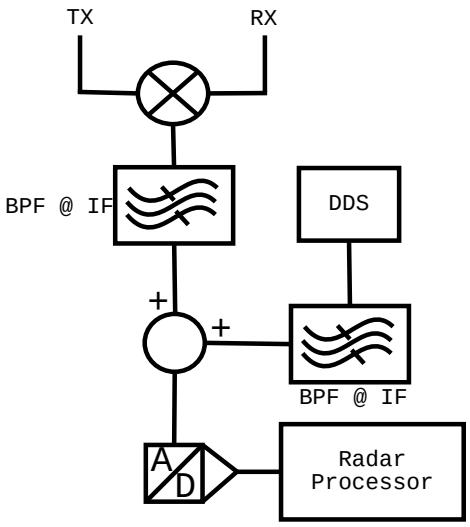


Figure 3.1: Simulation System Block Diagram

3. Transmit Frequency
4. Intermediate Frequency
5. Jitter (in RMS radians) of the TX and RX synthesizer
6. Clock Jitter in the cancellation signal.
7. Output precision (in bits) of the DDS.

The output of the function is the RMS error after subtraction of the cancellation signal from the IF signal.

3.2 Simulation Parameters

A large enough number of cycles needs to be specified to allow time for the filters to settle. It was observed that at least 2000 cycles of the TX signal was required to get stable results at IF, with 20 samples taken per TX cycle. The TX frequency was chosen to be 200MHz and the IF is 2MHz. This implies an RX frequency of 202MHz.

Jitter and Phase Noise

It is standard practice by clock source manufacturers to specify frequency stability in terms of phase noise. Since the system is simulated in the time domain, the phase noise characteristics (frequency domain) of the oscillators need to be converted to their time domain equivalent, namely period jitter.

The method described by Adler [2] was used to calculate the jitter for the TX and RX synthesizers from its phase noise curves, which were calculated using SimPLL [8]. The

file 'simulation.pll' on the compact disc named Appendix B contains the simulation parameters.

The same method was used in calculating the DDS jitter, which is directly obtainable from the system clock phase noise specification. A range of jitter values around those calculated was used for both parameters to determine the effect of increasing and decreasing phase noise in the system.

DAC Output Precision

Output precisions of 8, 10, 12, 14 and 16 bits were used to determine the effect of quantization noise. These values were chosen since they are standard for Digital-to-Analogue Converters (DAC).

3.3 Operation of Simulation

The TX and RX signals are generated using the parameters specified above and mixed, yielding

$$v(t) = \cos(2\pi f_{RX}t + \phi(t)) \times \cos(2\pi f_X t + \phi(t))$$
$$= \frac{1}{2}\cos(2\pi f_{IF}t + \phi_1(t)) - \frac{1}{2}\cos(2\pi(2f_{RX} + f_{IF})t + \phi_1(t)),$$

where $\phi_n(t)$ is the jitter function derived from the phase noise curve. In the simulation this is modelled by discrete random numbers with a Gaussian distribution of zero mean and standard deviation calculated as described in the above section. This seems to be the standard way of defining jitter parameters [50].

Now the signal is filtered with a bandpass filter at f_{IF} (i.e. 2MHz) with a bandwidth of 100kHz. If the filter response is given by $h(t)$, then this operation results in

$$v_{IF}(t) = v(t) \otimes h(t)$$
$$\approx \frac{1}{2}\cos(2\pi f_{IF}t + \phi_2(t))$$

Next, the signal is sampled at 4 samples per cycle with 16 bit precision. The samples are taken at the zero-crossings and at its maximum and minimum values. That is

$$[v] = \left[\cos(\phi_1),\ \cos(\frac{\pi}{2} + \phi_2),\ \cos(\pi + \phi_3),\ \cos(\frac{3\pi}{2} + \phi_4)\right]_{16},$$

where the square brackets denote quantization and ϕ_n refers to offsets from the ideal values due to phase noise. These samples are then output by the DDS at bit precisions ranging from 8 to 16 and filtered with an identical bandpass filter. Assuming the phases of the IF and cancellation signals can be aligned to achieve exact anti-phase, the RMS error

between the the two signals is now calculated, i.e.

$$\epsilon_{RMS} = \frac{1}{N}\sum_{n=1}^{N}(v_{IF}(n) - v_{canc}(n))^2\,,$$

where N is the total number of samples. This error is then the output of the simulation.

3.4 Limitations of Simulation

At this point it must be noted that the MatLab filter models take numbers in the range [0, $f_{sample}/2$] as input parameters to specify the filter cutoff frequencies. It was seen that the filters become unstable as one approaches a relative cutoff frequency of 0. For this reason there is a limitation on the sampling rate that can be chosen. This directly influences the degree of phase alignment that can be achieved after filtering and this variable could thus not be simulated properly. It was found experimentally that the best filter response vs sampling rate allowed for 0.5^0 resolution (or 720 samples per cycle).

An advantage of this is that the real DDS also has finite phase resolution of the order $0.5^0$of and will not be in perfect anti-phase to the feedthrough signal.

3.5 Simulation Results

The effect of quantization noise alone in the system is examined first. Note that this simulation assumes zero phase-noise (and hence zero jitter).

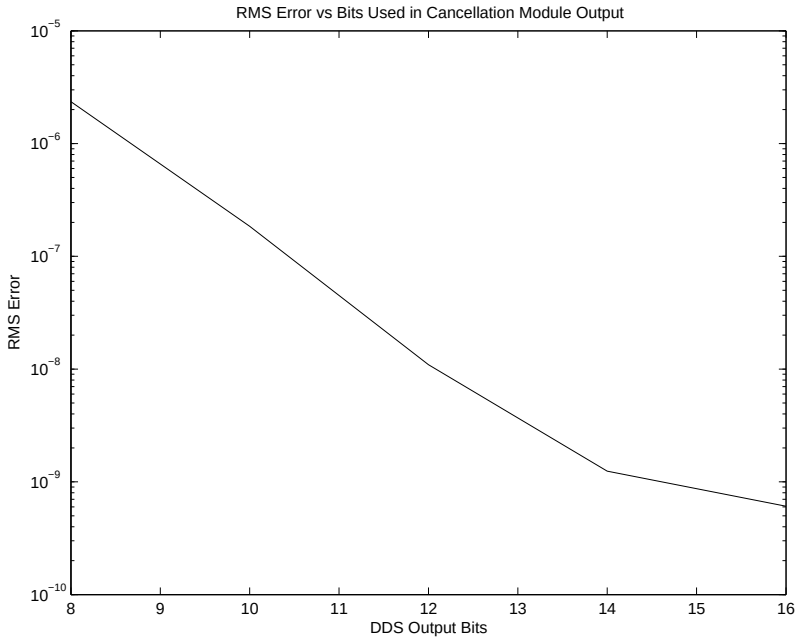


Figure 3.2: Effect of Quantization Noise on Cancellation

The simulation had samples taken at all points in the IF sinusoid and averaged. As is expected, the level of cancellation improves as the output resolution of the DDS is increased. It is seen in Figure 3.2 that the improvement becomes less drastic as one proceeds past 14 bits precision.

Next, jitter was included in both the TX and RX signals and in the Cancellation signal. Figure 3.3 shows the results.

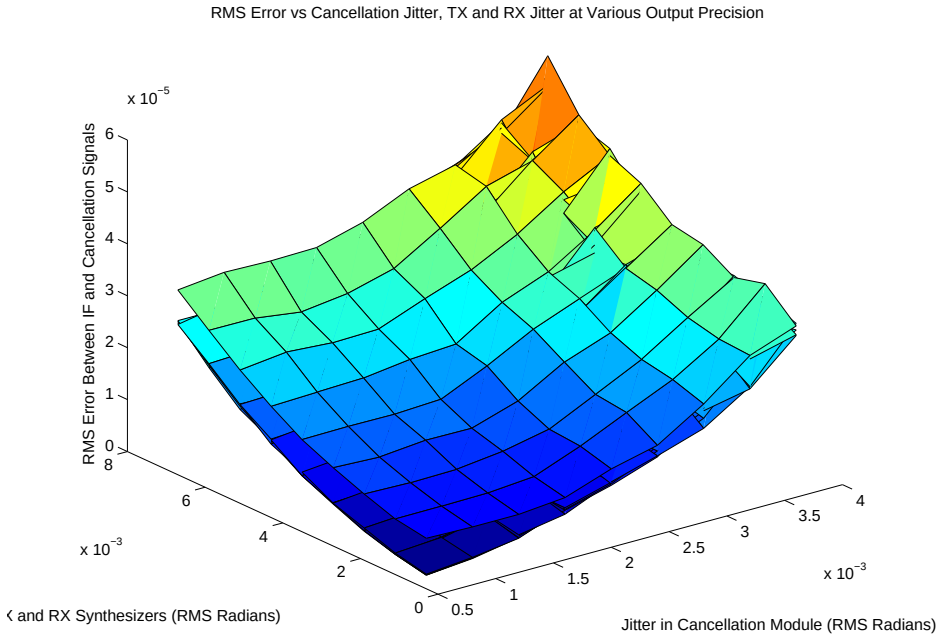


Figure 3.3: The Effect of Phase Noise and Quantization on Achievable Cancellation

There are five surfaces plotted in Figure 3.3, with only two being clearly visible. The surfaces represent different output precisions in the DDS. The upper visible surface represents 8-bit precision (representing the biggest RMS error), while the lower is a combination of 10, 12, 14 and 16 bits. It is seen that once realistic levels of phase noise are introduced to the system, negligible performance advantage is gained by using output precisions of more than 10 bits in the DDS.

The results of the simulation must be seen as conceptual, rather than absolute. The numerical results are less important than the finding that 10 bits of output precision in the DDS will provide almost identical cancellation to higher output resolutions.

3.6 Conclusions Drawn from Simulation Results

The following conclusions could be drawn from the simulation results:

1. A high degree of cancellation can be achieved if the cancellation module can be accurately calibrated. An RMS error between the leakage and cancellation signal of the order of $30\mu V$ was seen in Figure 3.3.

2. 10 bits amplitude and phase resolution in the DDS would achieve the same level of cancellation as higher bit resolutions in the presence of realistic levels of phase noise in the transmit, receive and cancellation synthesizers.

Chapter 4

Hardware Design and Basic Functional Testing

Chapter 4 contains a description of the hardware design process. The details will be kept to functional block-level, but should give the reader a good insight into what would be required to reproduce such a cancellation module. Detailed circuit diagrams are contained on the included compact disc named Appendix B.

The module takes the form of a 4-layer printed circuit board (PCB). Various considerations must be taken into account when designing a PCB to ensure a high degree of signal integrity and low electro-magnetic interference (EMI). The steps taken to ensure this are highlighted in this chapter. Test-software is also developed to verify the functionality of the module, but will not be used in the eventual radar system.

After testing the hardware, it could be concluded that the module fulfils all the functional requirement set out in the beginning of the chapter and operates as intended. It must be noted that some minor alterations could improve the operation of the module, but are not essential for its functionality.

4.1 Hardware Design Functional Requirements

The basic functional requirements for the IF Cancellation hardware are the following:

1. Generate a (single-ended) sinusoid of 2MHz. The method of generation must allow for near-instantaneous phase changes of the signal under the command of a controlling device.
2. Take as an input a differential IF signal of 2MHz.
3. Provide circuitry to convert the differential IF signal to a single-ended one.
4. Subtract the generated signal from the incoming IF signal, resulting in the cancelled signal.

5. Pass the cancelled signal through a digitally controllable gain-stage.

6. Make provision to select outputting either the incoming IF, the generated cancellation signal or the cancelled signal.

7. Convert the chosen single-ended output signal to differential, which is the final output of the circuit.

8. Provide an interface between the controller and the rest of the system via two bi-directional channels, clock and data. These channels must use the Low Voltage Differential Signalling (LVDS) standard.

The following section will describe how these basic requirements were met in hardware. Note that circuit-level details will not be given, but the explanations should allow the reader to recreate a similar device.

4.2 Meeting the Hardware Functional Requirements

The complete block-diagram of the designed IF Cancellation module is shown in Figure 4.1.

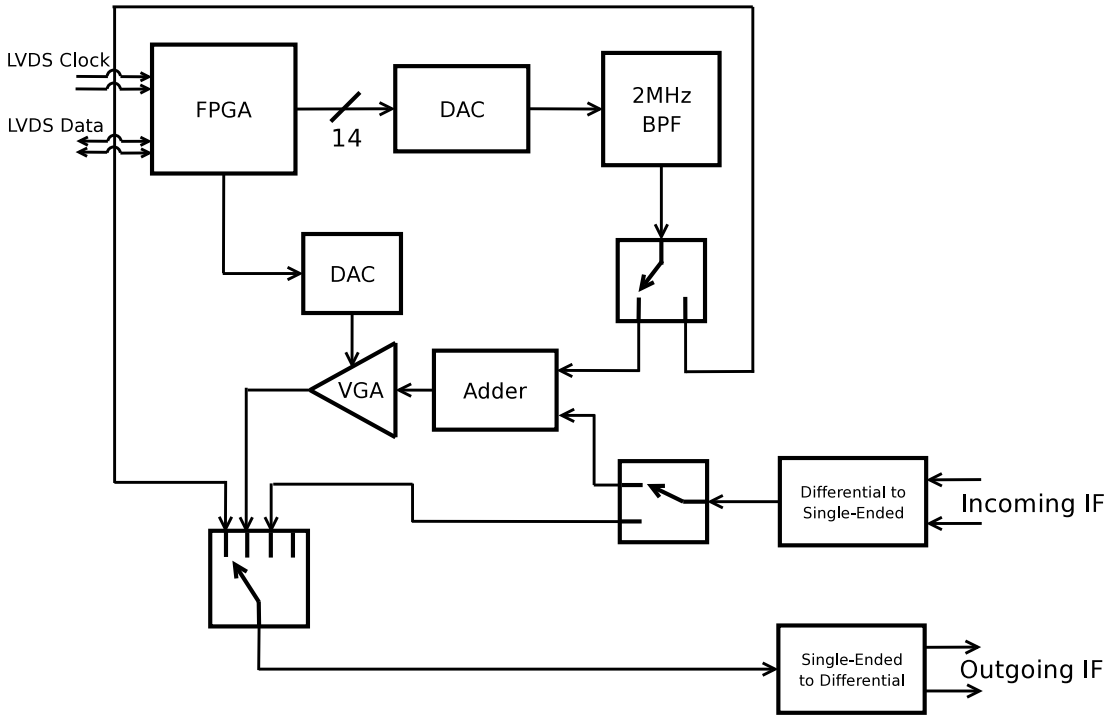


Figure 4.1: The complete block diagram of the IF Cancellation Module

The module was captured as a schematic, routed on a 4-layer PCB and sent off for manufacture. Note that control and clock signals from the FPGA to the DACs and switches are not shown to avoid cluttering the diagram.

The following sections will explain the objective of each of the functional blocks. For detailed circuit diagrams, the reader is referred to 'IFC.ddb' on the compact disc marked Appendix B.

4.2.1 Generating the Cancellation Signal

The most important consideration in the hardware design phase is which method to use in generating a 2MHz sinusoid. It was mentioned previously that Direct Digital Synthesis (DDS) is the only frequency generation technique that allows the rapid phase changes required by the system.

A review of off-the-shelf DDS ICs revealed that a 2MHz output is easily achievable. It showed that commercially available units are capable of bandwidths up to 400MHz and support a wide variety of on-chip modulation features, which is not required for this application. The units also have rather complex interfaces to external controlling devices and are expensive.

A more viable solution is to use a Programmable Logic Device (PLD) as a sinusoid lookup table (LUT) and to output its values to an external DAC. This is, in effect, results in the same system architecture as that of a simple DDS, without the unnecessary modulation features. The PLD can also be used as the controller in the circuit and provide the required bi-directional LVDS channels to the rest of the system. This approach will lower the cost and component count of the IFC and will hence be pursued.

The simulation of the system in Chapter 3 showed that output amplitude resolution above 10 bits achieves no improvement in the level of cancellation in the presence of realistic levels of phase noise in the clock source. Due to the negligible difference in price and level of circuit complexity between 10-bit and 14-bit DACs, a 14-bit DAC was chosen. This allows for a theoretical peak-signal-to-quantization-noise ratio of [56]

$$\left[\left(\frac{S}{N}\right)_{pk\,qnt}\right]_{dB} = 4.8 + 6m$$

$$= 88.8\,dB$$

The selected DAC has differential current outputs. It is recommended in Linear [45] and Analog [7] that an RF transformer with a 1:1 turns ratio be used to convert the DAC output to a single-ended voltage. The advantages of this approach include excellent rejection of common-mode distortion and wideband noise, as well as DC isolation. It is also easy to set the output impedance of the transformer by simply selecting a resistor value. This is of importance since the output from the transformer is connected to a bandpass-filter of a 50Ω input impedance which smoothes the discrete DAC output. Correct impedance matching ensures maximum signal-power transfer.

A Field Programmable Gate Array (FPGA) was chosen as the controlling device. The device directly supports bi-directional LVDS, thus no additional circuitry is required to provide the interface to the rest of the system. It also contains enough gates to store a high phase-resolution sinusoidal LUT, as well as the controlling firmware.

4.2.2 Converting Between Single-Ended and Differential Signals

The incoming IF signal is differential and needs to be converted to single ended in order to be added to the cancellation signal. Similarly, the IF signal selected to be output from the module needs to be converted from single-ended to differential. Differential signals are advantageous in that they offer a high degree of common-mode rejection. This will largely cancel noise from from high speed digital signals in the system that couple to the information carrying IF signals.

It is, however, more convenient to operate on single-ended signals. Commercial operational amplifiers are available that are specifically suited to converting between single-ended and differential signals. These operational amplifiers are used in the circuit and they require minimal external components.

4.2.3 Subtracting the Cancellation Signal from the Incoming IF

Cancellation is achieved by subtracting the generated cancellation signal from the incoming IF. Operational amplifier subtraction circuits require precise resistor matching [30] to achieve acceptable performance. An operational amplifier adder also needs accurate resistor matching, but consists of fewer resistors, so matching is simpler. The cancellation signal can be generated in exact anti-phase to the signal that needs to be cancelled and added, resulting in subtraction.

This approach was adopted, and a simple operational amplifier adder circuit was designed for the cancellation purposes.

4.2.4 The Variable Gain Stage

After cancellation has taken place, the resulting cancelled signal will be low in amplitude. This signal must now be amplified to the maximum input level of the data-capturing device: an ADC located elsewhere in the system. The level of amplification must be digitally controlled. Although there are digital variable gain amplifiers (VGAs) on the market, most of these products vary the amplification in 3dB steps. This is too coarse for the given application.

A better solution is to use an analogue VGA. An analogue VGA takes as input an analogue voltage to specify the gain in the circuit. This voltage can be generated by using a low-cost DAC, which is controlled by the FPGA (the controlling device in the circuit).

The combination of the DAC and the analogue VGA creates a gain stage that is finely adjustable via a digital input.

The VGA chosen consists of 2 stages and with correct circuit design, it is possible to vary the amplification ranges. This comes at a cost, however, as the bandwidth of the amplifier decreases as the gain configuration increases.

4.2.5 Creating a Selectable Output

It is required that the IF output from the cancellation module be selectable between the incoming IF (i.e. the signal goes straight through the circuit), the generated cancellation signal and the amplified cancelled signal. The selection must be digitally controlled by the FPGA. RF switches were used in an arrangement as shown in Figure 4.2.

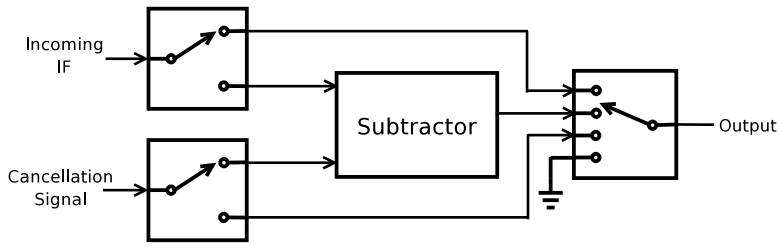


Figure 4.2: Switch configuration for IF Cancellation Module

The switches are controlled by the FPGA, which is not shown here. This is basically a more detailed version of the switch configuration shown in Figure 4.1.

4.2.6 Printed Circuit Board Design Considerations

The printed circuit board (PCB) is manufactured from FR-4 material and consists of four layers: 2 signal layers on the outside, a power plane and a ground plane. The signal integrity of the IF signals are of utmost importance in the radar system. Also, the quality of the digital signals on the board are paramount to establishing reliable communications with data-converters and external system modules.

Three of the main causes for degradation in signal integrity are discontinuities in the signal return path, power plane impedance and coupling from adjacent signals (crosstalk) [11]. Signal integrity problems are more critical in high-frequency designs, but simple measures can be taken to limit its effects in any circuit.

Providing Uninterrupted Signal Return Paths

Every electrical signal has a return path [12]. If there is a power or ground plane directly underneath the signal layer, the return path will make use of this plane to take the minimum impedance path with the smallest loop area [16]. This approach was adopted in the hardware design. The two centre layers of the PCB consists of power and ground planes.

It is also important that the plane is not split directly beneath the signal trace . In the case of an interrupted return path, the return current diverts to the smallest alternative loop path, usually passing through the nearest decoupling capacitor [38]. This causes huge impedance discontinuities and results in ground loops.

The PCB was laid out with the above facts in mind. As a result, all signal traces were routed to pass over solid planes.

Common Mode Noise in Differential Signals

The DATA, Clock, incoming and outgoing IF signals are differential pairs. Noise from external sources coupling into these channels will couple mutually into the pairs and can thus be seen as common mode noise. One of the reasons for using differential signals is that common mode noise is cancelled in differential receivers [30], thus providing a high level of signal integrity.

This measure largely takes care of crosstalk from adjacent signals, since the coupling is common to both signals in the differential pairs.

Guard Traces Surrounding Critical Signals

Benedict [10] suggests that guard traces be placed either side of the differential signals on the PCB. Guard traces are tracks that run parallel to the signal pairs and are connected to ground with vias at regular intervals. This reduces crosstalk by an order of magnitude [49].

Guard traces of twice the signal trace-width were placed one signal trace-width from the signal-carrying conductor on either side. This complies with the rules set out by Benedict [10].

Decoupling of Power Supplies

Decoupling of ICs ensures that varying instantaneous current demands can be met without causing a momentary fluctuation in the supply voltage. This is particularly crucial when using digital components.

Alexander [3] gives very complete guidelines for designing a Power Distribution System (PDS) using bypass/decoupling capacitors. The guidelines mostly pertain to high-speed systems, however. For the IF Cancellation Module, standard decoupling practice was used, namely placing 100nF capacitors as close as possible to each supply pin of each IC. Also, $22\mu F$ capacitors were used as decoupling for the power supplies.

4.3 Testing of Hardware

4.3.1 Testing Basic Functions with Test Software

Test software was developed in VHDL to be loaded onto the FPGA. The software had to test three functions:

1. The correct generation of a 2MHz sinusoid
2. The operation of the variable gain stage DAC
3. Toggling of the switches that route the output signal

Testing of the LVDS communication links is inherent, since the clock source for the FPGA comes from elsewhere in the system via the LVDS Clock link.

The 2MHz sinusoid was generated successfully. The resistor across the secondary winding of the transformer needed adjustment to ensure maximum signal-power transfer between it and the bandpass filter to which it is connected.

The variable gain stage works as intended. Data is written successfully to the gain-adjusting DAC by the FPGA. With the placement of certain resistors, the gain range can be altered. Maximum gain is 48dB.

The routing switches also operate correctly under control of the FPGA.

4.3.2 Testing Subtraction and Conversion Between Single-Ended and Differential Signals

The final tests for full hardware functionality involve verifying whether the single-ended to differential amplifiers (and vice-versa) and the subtraction/addition circuit work as planned. Both these functions can be verified with a single test that utilizes two IF Cancellation Modules.

One of the modules is configured to produce a 2MHz sinusoid, with the switches programmed to pass this generated signal directly through to the output. The second module now uses this signal as its IF input. The second module now also generates a 2MHz sinusoid and routes it, via the switches, to the input of the opamp adder. The incoming IF is also routed to the adder circuit.

After addition has taken place, the signal is passed through the variable gain stage and then to the single-ended to differential converter, which is the output of the circuit.

Initial attempts showed that the differential-to-single-ended amplifier went into saturation due to the DC-biased incoming IF signal. The DC-component was removed to some degree by the insertion of 100pF capacitors at the input of the amplifier. The signal was not a perfect sinusoid, but was of a high enough quality for testing purposes. Note that

this DC-blocking will not be required in the real system, since the incoming IF (coming from the RF demodulator) will not have a DC-component.

It could now be seen that all the components operate perfectly. The incoming and cancellation signals add as expected and the output amplitude can be controlled by the VGA. Due to shortcomings in the controlling software, the phase of either of the generated signals could not be changed, so the 180^{o} phase difference could not be achieved at this point. This will be tested in the following chapter, however, when the performance of the module is measured.

The single-ended amplified signal is correctly converted to differential by the final amplifier and output to the rest of the system. From this final test it can be concluded that all the hardware functional requirements have been met.

4.4 Conclusions About Hardware Design

Following the design and testing of the initial hardware, the following conclusions can be drawn:

1. All aspects of the hardware functions as intended.

2. Slight modifications can be made, namely adding more DC-blocking capacitors, especially in the IF signal paths. Although not required for operation in the system, it would facilitate easier testing of the hardware.

3. The signal integrity is at an acceptable level. No inter-module communication errors were encountered during the testing phase, and the DDS output has a SFDR of 70dBC (see Chapter 5) while noisy digital communications take place.

A second version of the hardware will be manufactured in the future that contains the modification mentioned above. In Chapter 5, the performance of the module will be tested and it will be shown that the hardware can successfully be integrated into the SFCW GPR for which it has been designed.

Chapter 5

Performance Measurements of IF Cancellation Module

In Chapter 5, the performance of the system will be evaluated. This phase measures the true success of the concept of IF cancellation and the hardware design.

First, spectral purity of the cancellation signal is measured. This measurement indicates that the DDS indeed generates a clean signal, with a narrowband Spurious-Free Dynamic Range (SFDR) in excess of 80dBC and wideband SFDR of 70dBC being measured. The phase noise of the generated signal is also measured here, and a plot of this measurement is included.

The second, and more important measure, relates to the level of cancellation that can be achieved. Two IF Cancellation Modules were used for this test - one generating an IF and the other generating a cancellation signal that is added to the IF. The test indicated that the possible cancellation exceeds 53dB and that the RMS error between the two signals is smaller than 4mV when the optimum phase difference and amplitude balance is achieved.

After the measurements are taken, the results are compared to those obtained from simulation. The comparison will show that the simulation model was accurate in its predictions pertaining to digital word lengths of amplitude and phase, but incorrect in predicting the RMS error between the IF and cancellation signals..

5.1 Output Spectrum of the DDS

First, the output spectrum of the DDS is measured using a Agilent E4407B spectrum analyzer. A plot of the spectrum of the 2MHz signal with a frequency span of 10MHz is shown in Figure 5.1.

As can be seen, spurious frequency components are present at harmonics of the fundamental frequency. This is consistent with theoretical predictions made in Chapter 2 relating to common DDS output spectra.

Shown in Figure 5.2 is a narrowband spectral plot with a width of 100kHz, the width

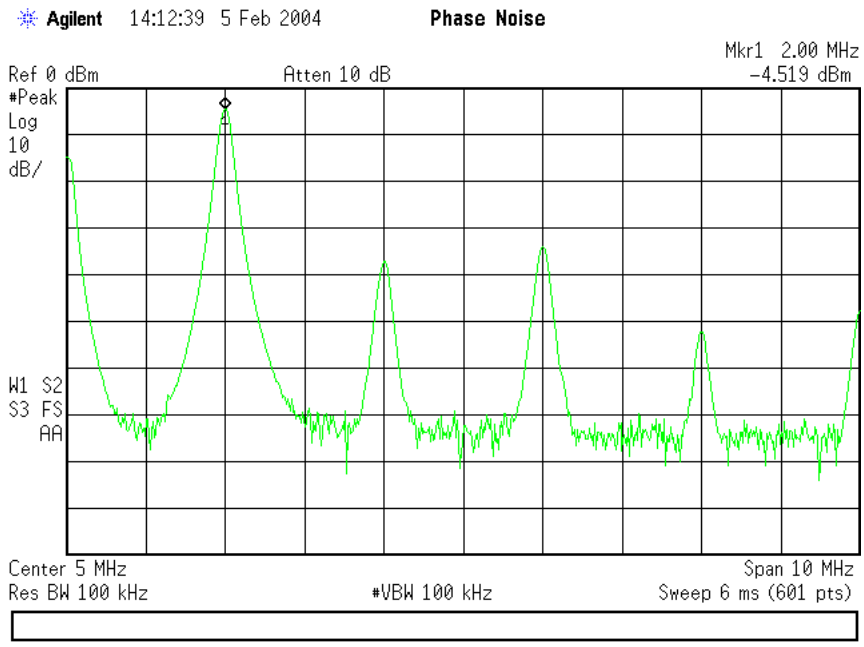


Figure 5.1: The frequency spectrum of the DDS output as measured by the Agilent E4407B spectrum analyzer

of 100kHz chosen to be the same as passband the IF bandpass filter. This measures the narrowband Spurious Free Dynamic Range (SFDR).

This spectral plot shows that this DDS system has a narrowband SFDR (in a 100kHz window around the carrier) of 85dBC with spurs present at the edges ($\pm$50kHz from carrier) of the spectral plot. A plot of the wideband SFDR, measured from DC to the Nyquist rate ($f_{clk}/2$) , is seen in Figure 5.3.

The wideband SFDR is seen to be 70dB. A review of commercially available integrated DDS devices revealed that this figure is better than most of the competing devices, and of the same order as those of high quality devices. This has partly to do with the fact that a 2MHz signal is generated from an 8MHz clock, leaving no phase truncation and hence minimum spurs.

5.2 Phase Noise Measurement of the DDS

Phase noise was measured using the Agilent E4407B spectrum analyzer in “phase noise mode”. The frequency offset starts at 10Hz (the smallest offset available on the equipment) and ends at 100kHz. The upper limit was set at 100kHz to coincide with the bandwidth of the IF filters. A plot of the measured phase noise is shown in Figure 5.4.

This plot is now compared with that of the clock driving the FPGA that controls the DDS system. The two phase noise specifications are given in tabular form in Table 5.1.

As can be seen, the small-offset phase noise of the DDS is better than that of the clock, but gets worse as the frequency offset is increased. This is inconsistent with the prediction

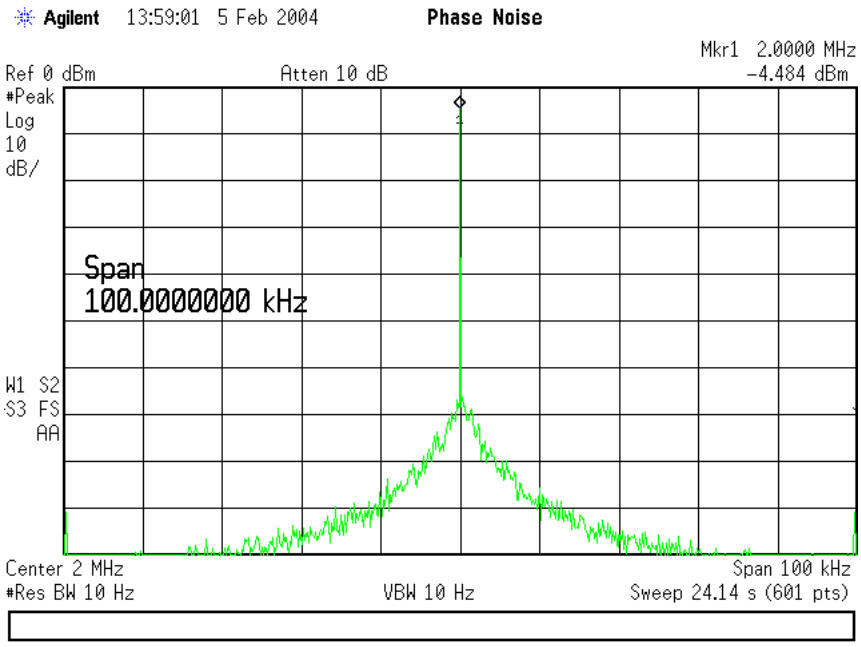


Figure 5.2: Narrowband spectral plot of the DDS

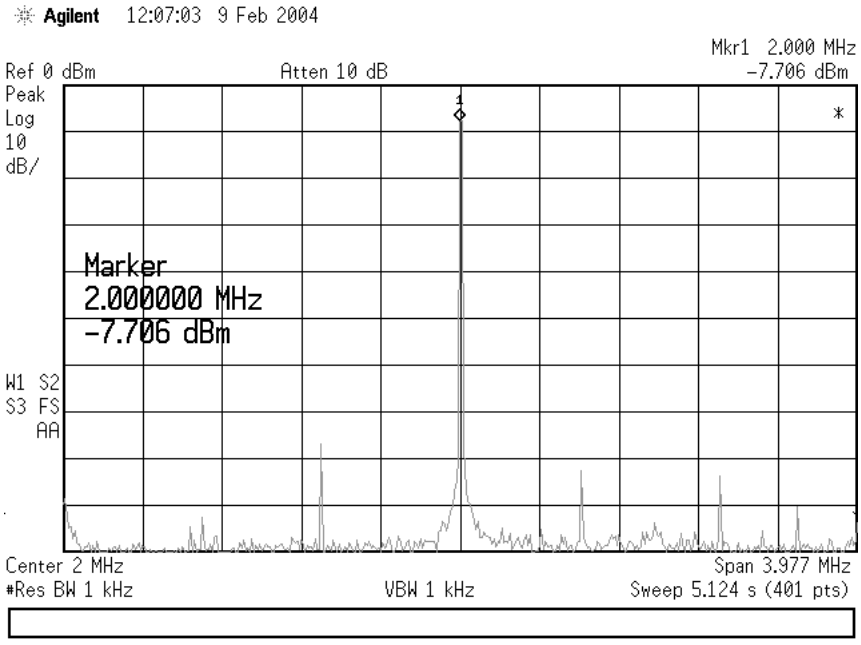


Figure 5.3: Narrowband spectral plot of the DDS

Table 5.1: Phase noise measured from DDS

Offset from Carrier (Hz)	Clock Source Phase Noise (dBC)	Phase Noise Reading (dBC)
10	65	80
100	105	82
1000	128	80
10000	142	100
100000	141	120

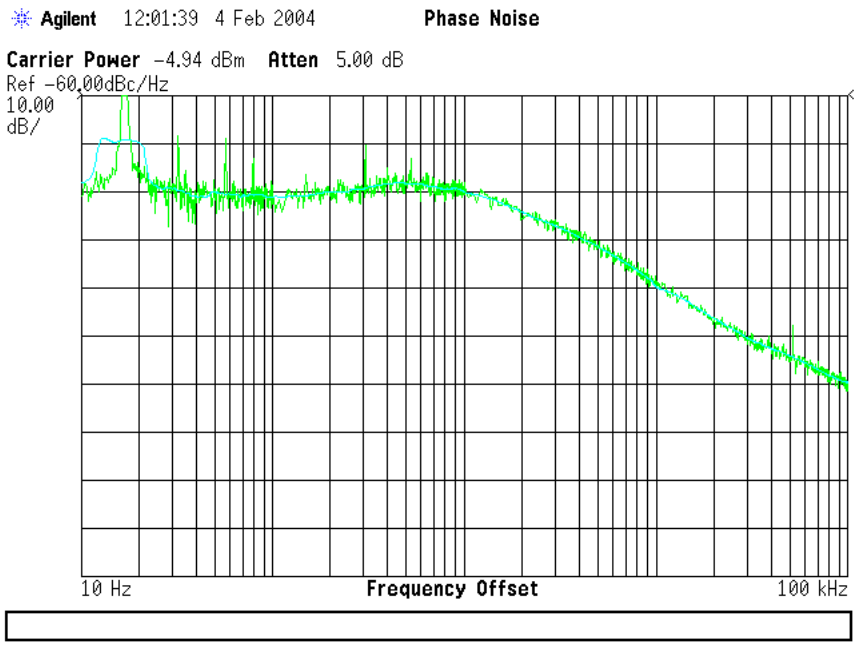


Figure 5.4: Phase noise plot of the designed DDS

that DDS phase noise will match or better that of its clocking source. A possible reason for this is the fact that the FPGA introduces variable delay times on the digital outputs. This is equivalent to adding jitter to the clock source and an hence increases phase noise. This jitter is present in the FPGA that produces the clock for the DDS, as well as in the clock that drives the output DAC of the DDS. Although not as good as that of the clock, the phase noise performance of the DDS system is reasonable when compared to commercially available DDS units.

5.3 Measuring Cancellation Capabilities of the IF Cancellation Module

In this final test section, the level of cancellation that can be achieved will be measured. Two IF Cancellation Modules were used for this test, producing two sinusoids. The amplitudes of the two signals were balanced first. After this, the phase of one of the signals was adjusted to attempt to achieve a 180^{O}phase difference between them. It was seen that using more than 10-bit phase resolution in the DDS phase accumulator did not result in better cancellation. The phase was thus set to $\frac{360^o}{2^{10}} = 0.35^o$ accuracy.

Shown in Figure 5.5 and Figure 5.6 are the spectra of the IF and the cancelled signals, respectively. It was measured using the Agilent E4407B spectrum analyzer. The span is once again set to 100kHz.

As is seen, cancellation of 53.7dB is achieved. This figure is measured after the the system has been running for approximately 30 seconds, since it then reaches stability.

It must be noted that the cancellation is temperature dependent and decreases as ambient

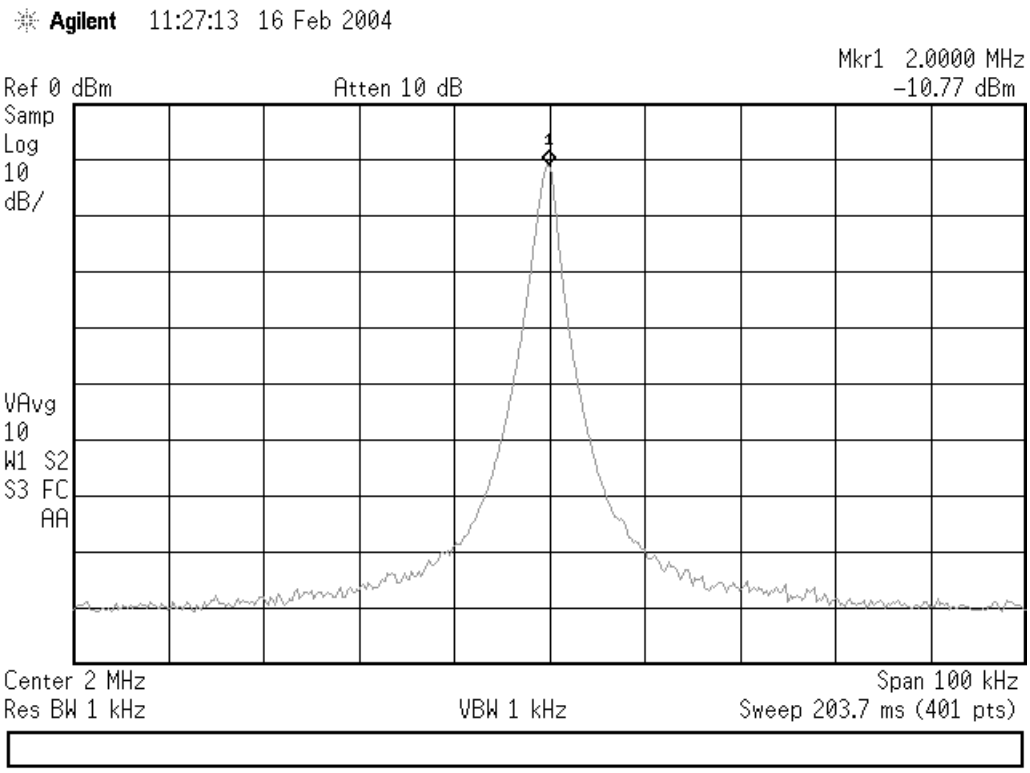


Figure 5.5: The output spectrum of the IF signal

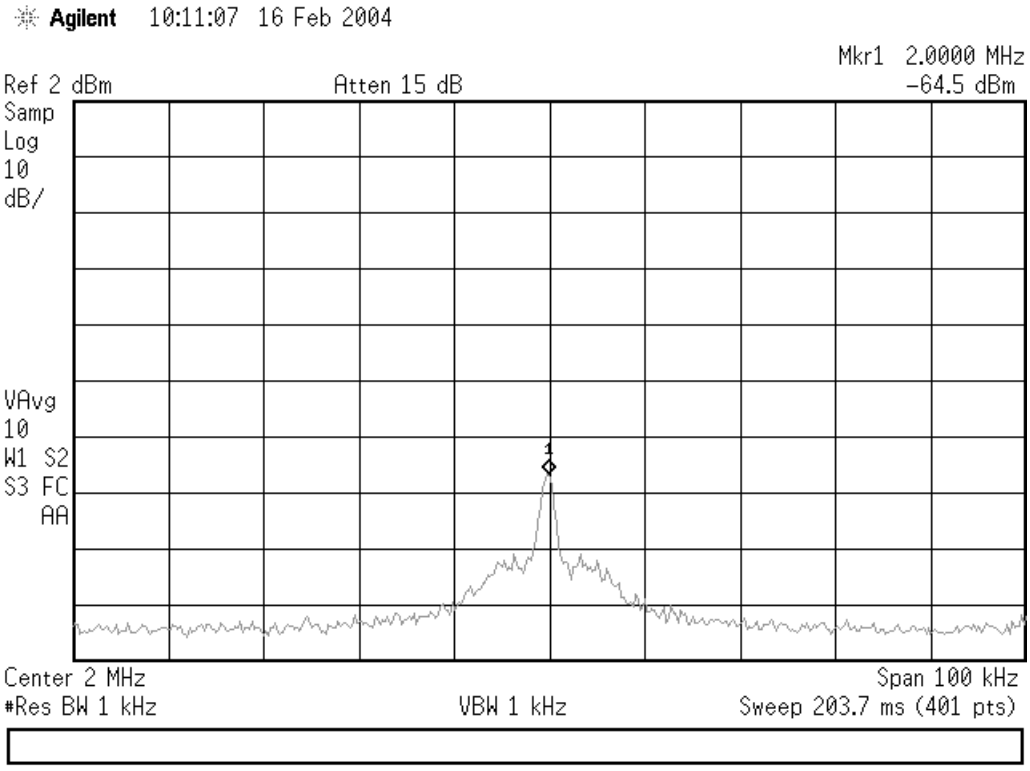


Figure 5.6: The spectrum of the cancelled signal

temperature increases. Also, cancellation in the eventual radar system will be slightly reduced from the measured result here, since the phase noise between the two signals will not be correlated as is the case here.

Next, the RMS error between the two signals was measured using a Hewlett Packard 54645D Oscilloscope. The scope was set to measure the RMS voltage of the subtracted signal. Once again, the result was dependent on the ambient temperature, but at room temperature, an RMS error of 3.9mV was registered. This result is adequate if one considers that the noise in the system exceeds 2.6mV RMS when no signals are present.

5.4 Review of Measured and Simulation Results

A comparison between the simulation and measured results can now be presented.

In Chapter 2 it was shown through simulation that no signal-to-noise advantage is gained by using more amplitude than phase bits or *vice versa* in the DDS architecture. Furthermore, it was shown in Chapter 3 that 10-bits amplitude resolution in the DDS would achieve similar cancellation results than higher bit-resolutions in the presence of realistic levels of oscillator phase noise. In attempting to achieve exact anti-phase between the IF and cancellation signals earlier in this chapter, it was found that 10-bits phase resolution achieved the same cancellation as using more bits in the phase accumulator.

This implies that the simulation of Chapter 3 is correct, since it indicated that 10-bits amplitude resolution would achieve maximum possible and it was found in practice that using more than 10-bit phase-resolution did not improve cancellation. In other words, the simulation findings in chapters 2 and 3 are correct and one can conclude that the developed model is conceptually accurate.

On the other hand, there is a significant difference between RMS error predicted and that which was measured. Simulation indicated that the RMS error would be about 30μV, whereas 3.9mV was measured. This discrepancy could be due to 3 factors

1. The bandpass filters could not be accurately modelled in MatLab
2. System noise due to analogue components and Electro-Magnetic Interference (EMI) from adjacent electronic devices were not included in the model.
3. Passive components have unpredictable tolerances and slight mismatches of components in crucial circuits, such as the operational amplifier summer, will cause a degradation in performance.

These factors are not trivial to include in this model, but could serve as recommendations for similar projects in the future.

In terms of the SFCW GPR system for which this device is intended, it shows that the instantaneous dynamic range of the system can theoretically be increased by 53.7dB with

the use of the IF Cancellation Module. This relies on the fact that the device can be accurately calibrated to efficiently cancel each of the stepped frequencies mixed down to IF. A lookup-table would have to be created that contains the phase offset and amplitude information of each of the mixed-down transmit frequencies.

Chapter 6

Conclusions

This final chapter is an overview of this paper and will draw conclusions from the results obtained during this dissertation. The most important of these conclusions is that the concept and physical incarnation of an IF Cancellation Module gives promising results. A high degree of cancellation is possible with the module and, with correct calibration, could dramatically improve the instantaneous dynamic range of the SFCW GPR for which it has been designed.

Conclusions Drawn from Dissertation

The objective of this dissertation was to simulate, design and implement an IF Cancellation Module that could be used to cancel the direct coupling signal between the transmit and receive antennas in a Stepped Frequency Continuous Wave Ground Penetrating Radar. The method of cancellation involves accurately recreating this leakage signal and subtracting it from the returned radar signal. This cancellation would increase the effective instantaneous dynamic range of the data-capturing device, an analogue-to-digital converter (ADC), since this large unwanted signal usually uses most of the ADCs input range. It was seen in a simulation that if multiple scans (stacking) is used to identify a target through integration, less integration time is needed if the leakage signal is cancelled.

Direct Digital Synthesis (DDS) was chosen as the method of recreating the leakage signal, due to its ability to rapidly change the phase of its output sinusoid. The operation of DDS and its shortcomings was discussed in Chapter 2. Phase noise in signal sources was also covered in this chapter, since all the synthesizers in the SFCW GPR will have frequency instability which will influence the degree of cancellation that can be achieved. Simulations at the end of this chapter showed the deterioration in signal quality if phase and amplitude errors exist between the IF and the cancellation signals. Phase noise was also introduced in the simulation.

Chapter 3 shows the development of a model for the cancellation device. The model takes phase noise in the various clock sources, quantization noise in the DDS and phase

errors into account. The model is used to simulate the device in MatLab. Chapter 4 contains descriptions of the hardware design issues, without giving circuit level details. The chapter also shows basic tests that were performed to verify that the hardware functioned correctly.

In Chapter 5 it is shown that the device achieves high levels of cancellation (53dB) and it is proven that the device could indeed be used to increase the dynamic range of the radar system if it is correctly calibrated.

The most important conclusions that could be drawn from this study are:

1. The concept of IF Cancellation using direct subtraction of the leakage signal in a Continuous Wave radar is viable. After careful adjustment of amplitude and phase of the cancellation signal, 53.7dB cancellation could be achieved. If the phase and amplitude of the cancellation signal could be calibrated to cancel the entire band of transmit frequencies in the SFCW GPR, an improvement in instantaneous dynamic range of the order of 50dB can be achieved in the radar system.

2. The designed hardware functioned as intended, although slight modifications could be made to simplify testing of the circuit

3. The Direct Digital Synthesizer that was designed to generate the cancellation signal performs as well and better than commercially available devices in terms of spectral purity. Narrowband SFDR was measured at 85dBC and wideband SFDR was seen to be 70dBC. Jitter introduced by the FPGA does, however, cause a deterioration in the phase noise characteristic of the DDS compared to its clocking source.

4. The simulation model developed is conceptually correct and could be used as an aide in the hardware design process. It correctly predicted that 10-bit amplitude resolution in the DDS would achieve as effective cancellation as higher bit-resolutions due to phase noise in the oscillators. It was also predicted that no improvement in signal-to-noise ratio is achieved by using more amplitude bits than phase bits in the DDS or *vice versa.* These predictions complemented each other when it was found in practice that no cancellation improvement is gained by using more than 10-bit phase

   It was seen, however that the simulation was numerically inaccurate, since an RMS error between the IF and cancellation signal of 30μV was predicted, while 3.9mV was measured. Various factors could be responsible for this, most likely the absence of circuit noise in the model.

5. A summary of the most important measured quantities is given in 6.1 :

Table 6.1: Summary of Measured Results

Narrowband SFDR (100kHz)	85dBC
Wideband SFDR	70dBC
DDS Phase Noise at: 10Hz	80dBC
100Hz	82dBC
1kHz	80dBC
10kHz	100dBC
100kHz	120dBC
Maximum Cancellation	53.7dB
Best Achieved RMS Error	3.9mV
RMS System Noise	2.65mV

Appendix A

This appendix contains an example of how to calculate jitter from a phase noise specification or plot as shown in [50]. It must be noted that a scaling factor of unknown origin is used in the calculation. Correspondence with the author of the article did not clear up the mystery. The method was chosen, however, because it gives the most plausible results.

The validity of the calculation was verified by comparing the jitter result obtained from a phase-noise specification with the same signal source's quoted jitter figure.

Consider the phase noise plot shown below, taken from a oscillator manufacturer.

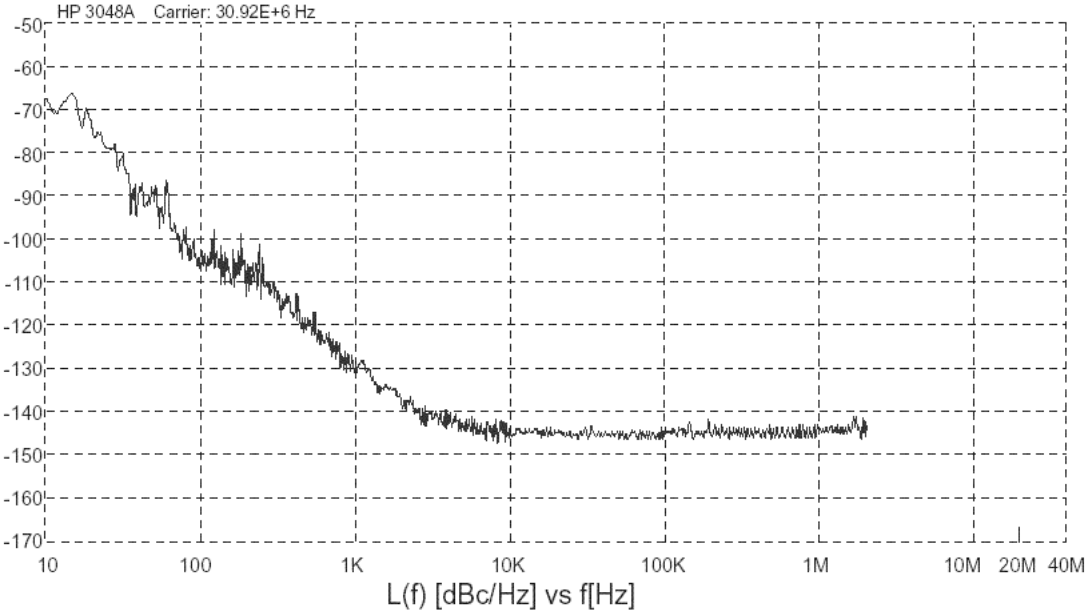


Figure 1: Phase noise plot of an oscillator

The plot needs to be integrated and the bandwidth of integration must be specified. In this case, assume the bandwidth is 1MHz. The first step is to identify the different slopes on

the graph, as defined in Chapter 2 of this paper Also, the power levels need to be converted to watts. In the above example, the following information can be seen:

Table 2: Phase noise information of specification given above

Offset	Power (dBC)	Power (W)	Approximate Slope
10Hz	65	316.2×10^{-12}	$\frac{1}{f^4}$
100Hz	105	32×10^{-15}	$\frac{1}{f^2}$
1kHz	128	158×10^{-18}	$\frac{1}{f^2}$
10kHz	144	4×10^{-18}	$\frac{1}{f^0}$
100kHz	144	4×10^{-18}	$\frac{1}{f^0}$
1MHz	144	4×10^{-18}	$\frac{1}{f^0}$

Now, integration of the individual curve sections is done. Note the correction factor - it is the lower limit of integration to the power of the slope in that part of the curve. Thus

$$p_1 = 316.2 \times 10^{-12} \times 10^4 \int_{10}^{100} \frac{1}{f^4} df = 1.05 \times 10^{-9}$$

$$p_2 = 32 \times 10^{-15} \times 10^4 \int_{100}^{1000} \frac{1}{f^2} df = 2.88 \times 10^{-12}$$

$$p_3 = 158 \times 10^{-18} \times 10^6 \int_{1kHz}^{10kHz} \frac{1}{f^2} df = 1.422 \times 10^{-13}$$

$$p_4 = 4 \times 10^{-18} \times 1 \int_{10kHz}^{1MHz} \frac{1}{f^0} df = 3.96 \times 10^{-12}$$

Now, the power contributions are summed, giving

$$P_{tot} = p_1 + p_2 + p_3 + p_4$$

$$= 1.05698 \times 10^{-9}\, watts$$

To proceed, this number is now converted back to dBm. This gives $P_{dBm} = -59.8dBm$. Now the RMS jitter can be calculated in various units, depending on the application. RMS Jitter in degrees is

$$J_{RMS\,degrees} = \frac{360}{2\pi} \times 10^{\frac{-59.8}{20}}$$

$$= 0.059^o$$

If the frequency of the oscillator is known, the RMS Jitter can be calculated in seconds.

Assume a clock frequency of 32MHz:

$$J_{RMS\,seconds} = \frac{J_{RMS\,degrees}}{360 \times 32 \times 10^6}$$

$$= 5.09\,picoseconds$$

This result coincides with the oscillator jitter specification of 6ps RMS jitter maximum.

Appendix B

Please refer to the attached CD.

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